Panchip Microelectronics Co., Ltd.

PAN1020

Datasheet

BLE SoC Transceiver

Version: 1.7

Release date: Qct. 2020

Shanghai Panchip Microelectronics Co., Ltd.

Address: The 3rd Floor of Building D, No. 666 Shengxia Road
Zhangjiang Hi-Tech Park, Shanghai
People's Republic of China

Tel: 021-50802371

Website: http://www.panchip.com

USING THIS DOCUMENT

The information in this document is subject to change without notice. Every effort has been made in the preparation of this document to ensure accuracy of the contents, but all statements, information, and recommendations in this document do not constitute a warranty of any kind, express or implied.

TRADEMARKS

Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

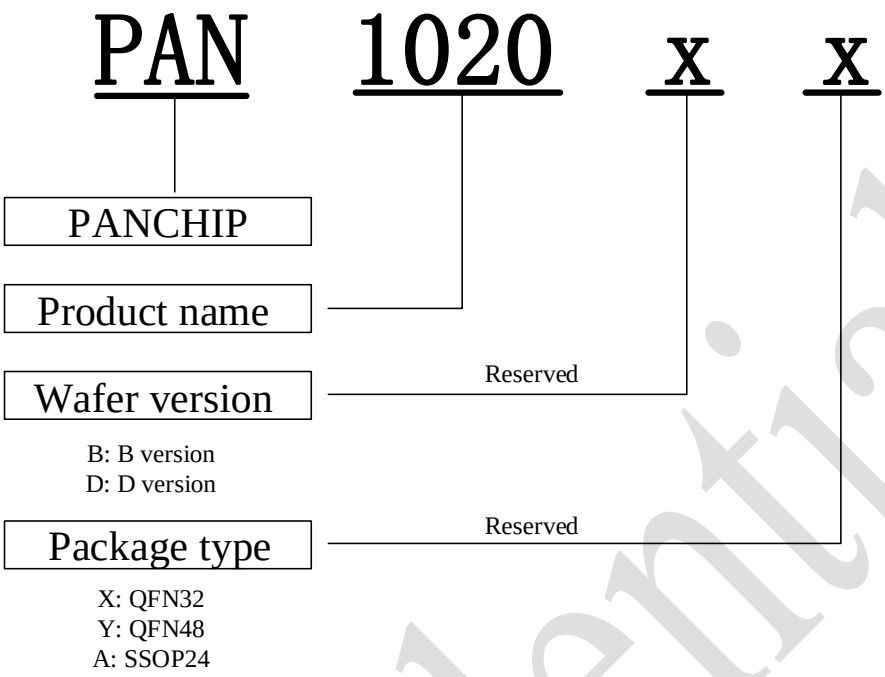
DISCLAIMER

All or part of the products, services and features described in this document may not be within the purchase scope or the usage scope. Unless otherwise specified in the contract, all statements, information, and recommendations in this document are provided "AS IS" without warranties, guarantees or representations of any kind, either express or implied.

REVISION HISTORY

Version	Date	Content	Reference
1.0	Nov.2017	Initial	《PAN163CX Datasheet_V1.2-EN》
1.1	Jul. 2018	Add the pin description of QFN 48-PIN Complement the pakage dimension of the QFN 48-PIN	-
1.2	Dec.2018	Refresh parts of the parameter of “ELECTRICAL CHARACTERISTICS” Modify the description of “Feature” Add the charpter of “PRECAUTIONS”, “STORAGE CONDITIONS” and “CONTACT US”.	-
1.3	June.2019	Add the SSOP24 package.	-
1.4	Oct.2019	Update the SSOP24 application reference circuit	-
1.5	Dec.2019	Update the electrical characteristics of ADC.	-
1.6	Jul.2020	Add “4.5 Digital Input/Output Characteristics”.	-
1.7	Qct.2020	1) Add “Naming Rules” and “Product Series” 2) P1.1 of PAN1020DY has no actual function, P1.1 of PAN1020BY has actual function.	-

Naming Rules



Product Series

Product series	Wafer version	Package	GPIO	UART	SPI	I2C	PWM channel	ADC channel	ADC range(V)
PAN1020BX	B	QFN32	25	2	3	2	8	8	0.4~2.4
PAN1020BY	B	QFN48	41	2	3	2	8	8	0.4~2.4
PAN1020BA	B	SSOP24	15	2	3	2	4	4	0.4~2.4
PAN1020DX	D	QFN32	25	2	3	2	8	8	0~2.4
PAN1020DY	D	QFN48	40	2	3	2	8	8	0~2.4
PAN1020DA	D	SSOP24	15	2	3	2	4	4	0~2.4

Contents

List of Figures

List of Tables

Abbreviation

ADC	Analog-to-Digital Converter
ATT	Attribute Protocol
BER	Bit Error Rate
BLE	Bluetooth Low Energy
BOD	Brown-out Detector
CPU	Central Processing Unit
DMA	Direct Memory Access
FIFO	First Input First Output
GAP	Generic Access Profile
GATT	Generic Attribute Profile
GPIO	General-purpose I/O
HID	Human Interface Device
HXT	High speed crystal oscillator
I2C	Inter—Integrated Circuit
IAP	In-Application-Programming
ICP	In-Circuit Programming
ISP	In-System Programming
L2CAP	Logical Link Control and Adaptation Protocol
LDO	Low dropout regulator
LIRC	Low speed RC oscillator
LVR	Low Voltage Reset
LXT	Low speed crystal oscillator
MCU	Microcontroller Unit
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RAM	Random access memory
SM	Security Manager
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver/Transmitters
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

1 General Description

The PAN1020 integrated circuit has a fully integrated radio transceiver and baseband processor for Bluetooth Low Energy. It can be used as an application processor as well as a data pump in fully hosted systems.

The PAN1020 contains an embedded Flash memory for storing Bluetooth profiles as well as custom application code. The qualified BLE protocol stack, stored in a dedicated Flash area, as well as the customer application software run on the embedded MCU processor. Low leakage Retention RAM is used to store all the sensitive data and connection information while in Deep Sleep mode.

The BLE firmware includes the L2CAP service layer protocols, Security Manager (SM), Attribute Protocol (ATT), the Generic Attribute Profile (GATT) and the Generic Access Profile (GAP). Furthermore, application profiles such as Proximity, Health Thermometer, Heart Rate, Blood Pressure, Glucose and Human Interface Device (HID) are supported.

The MCU part of PAN1020 is the 32-bit microcontroller. It supports a wide range of applications from low-end, price sensitive designs to computing-intensive ones and provides advanced high-end features in economical products.

The PAN1020 has many high-performance peripheral functions, such as general purpose I/O port(25 GPIOs for QFN32 package, 40 GPIOs for PAN1020DY, 41 GPIOs for PAN1020BY and 15 GPIOs for SSOP24 package), three 32-bit timers, two UARTs, two group SPI interfaces, two I2C interfaces, one 16-bit PWM generators providing eight channels, an 8-channel 12-bit ADC, Watchdog Timer, Window Watchdog Timer, and a Brown-out Detector. All these peripherals have been incorporated into the PAN1020 to reduce component count, board space and system cost.

Additionally, the PAN1020 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product. PAN1020 also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

The PAN1020 can run up to 52 MHz and operate at a wide voltage range of 2.2V ~ 3.6V and temperature range of -40℃ ~ +85℃. For PAN1020, the embedded FLASH size up to 256 Kbytes and SRAM up to 16 Kbytes. It also offers size configurable Data Flash (shared with program flash), and configurable flash size for the ISP.

1.1 Key Features

- **BLE**
  - Bluetooth 4.2 support
  - Bluetooth SIG Mesh support
- **RF**
  - 2.4GHz RF transceiver
  - RX sensitivity: -90 dBm@1Mbps
  - Maximum received signal: 0 dBm
  - Programmable TX output power: 13 dBm(Maximum), 8 dBm(Typical)
  - Single wire antenna: no RF matching or RX/TX switching required

- **Core**
  - MCU core running up to 52 MHz
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
- **Memory**
  - 256 KB Flash memory for program memory
  - 16 KB SRAM
- **Peripheral**
  - QFN32 package
    - 25 GPIOs
    - Two UARTs
    - Three SPIs
    - Two I2Cs
    - One 8-channel ADC
    - One 8-channel PWM0
  - QFN48 package
    - 41 GPIOs for PAN1020BY, 40 GPIOs for PAN1020DY
    - Two UARTs
    - Three SPIs
    - Two I2Cs
    - One 8-channel ADC
    - One 8-channel PWM0
  - SSOP24 package
    - 15 GPIOs
    - Two UARTs
    - Three SPIs
    - Two I2Cs
    - One 4-channel ADC
    - One 4-channel PWM0
  - Three channel 32-bit Timers (one 8-bit pre-scaler counter with 24-bit up-timer for each timer)
  - DMA up to 3 channels (one per source and destination pair)
  - Two UART devices with DMA
  - Two Group SPI master and slave devices with DMA
  - Two I2C master and slaver devices with DMA
  - 12-Bit ADC with Eight Channels
  - One built-in 16-bit PWM generators with eight channels
  - One WDT with 18-bit up counter
  - One WWDT with 6-bit down counter value (CNTDAT) and 6-bit compare value (CMP-DAT)
- **Special features**

- ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In Application Programming)
- BOD (Brown-out Detector) threshold levels: 2.87V/2.72V/2.34V/2.06V
- 96-bit unique ID
- LVR (Low Voltage Reset) threshold voltage level: 1.7±0.1V

- **Package**
  - QFN32 package, 5 × 5 mm
  - QFN48 package, 6 × 6 mm
  - SSOP24 package, pin pitch = 0.635mm
- **DC/AC Charactaristics**
  - Operating Temperature: -40℃~85℃
  - Operating voltage: 2.2~3.6V
  - Reliability: ESD HBM pass ±2KV
  - Built-in LDO for wide operating voltage: 2.2V to 3.6V
    - ~2uA @ deep sleep mode, wake up by internal 32K oscillator

1.2 Typical Applications

- TV and STB remote control
- Wireless mouse and keyboard
- Wireless gamepads
- Smart home automation

2 Block Diagram

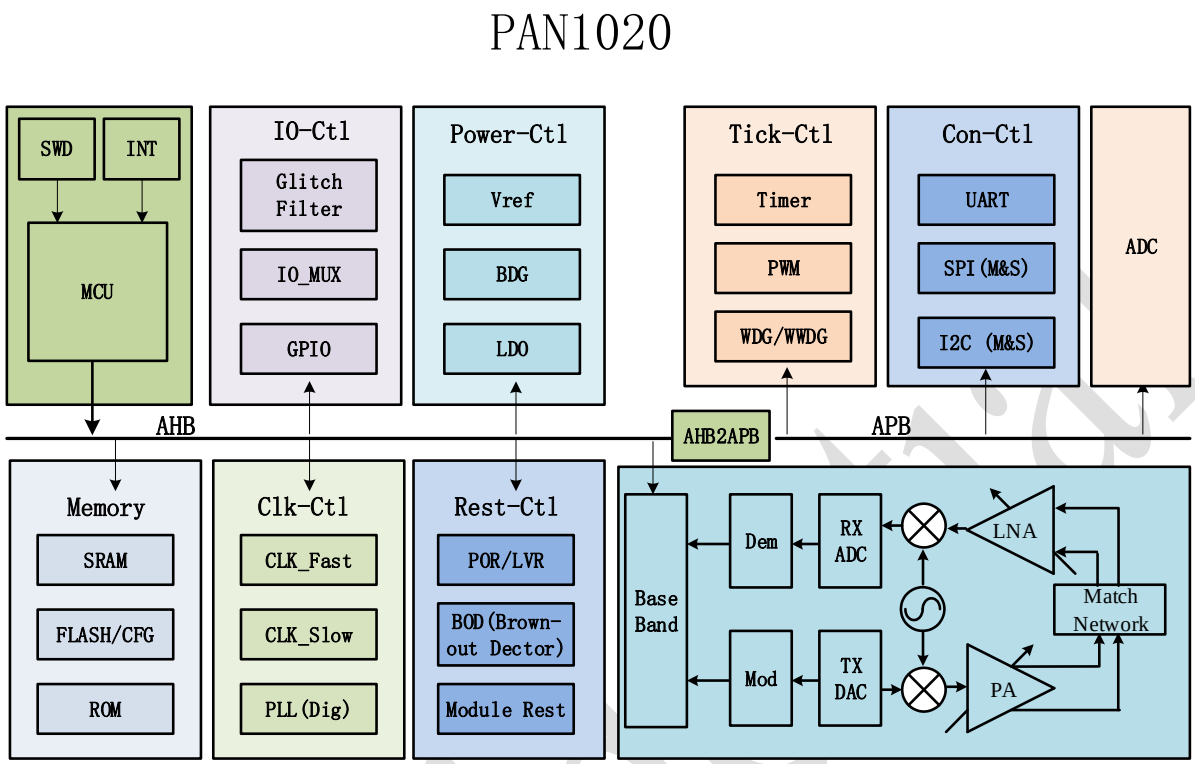


Figure 2-1 PAN1020 Block Diagram

3 Pin Information

3.1 QFN 32-PIN Diagram

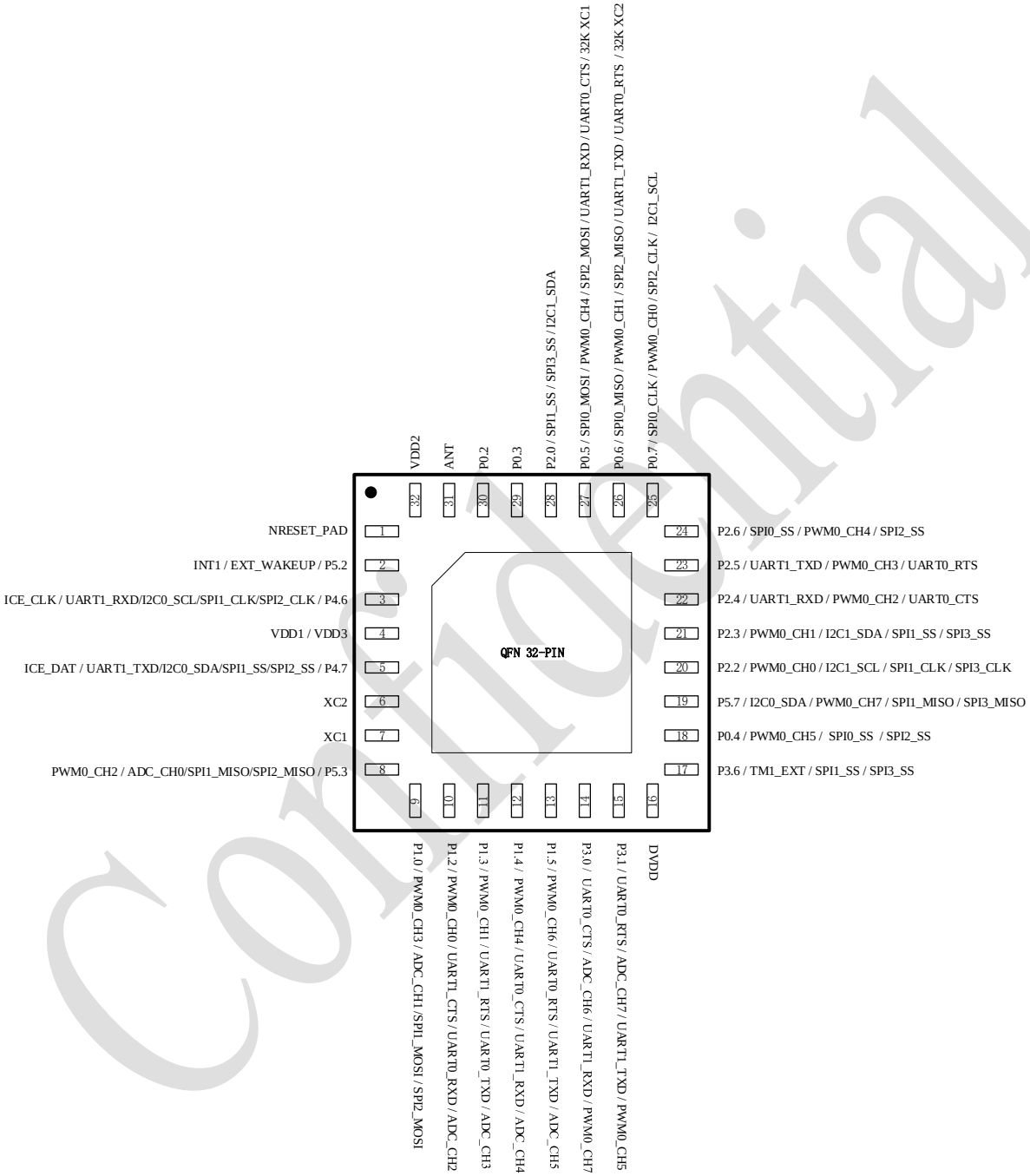


Figure 3-1 PAN1020 QFN 32-PIN Diagram

3.2 QFN 48-PIN Diagram

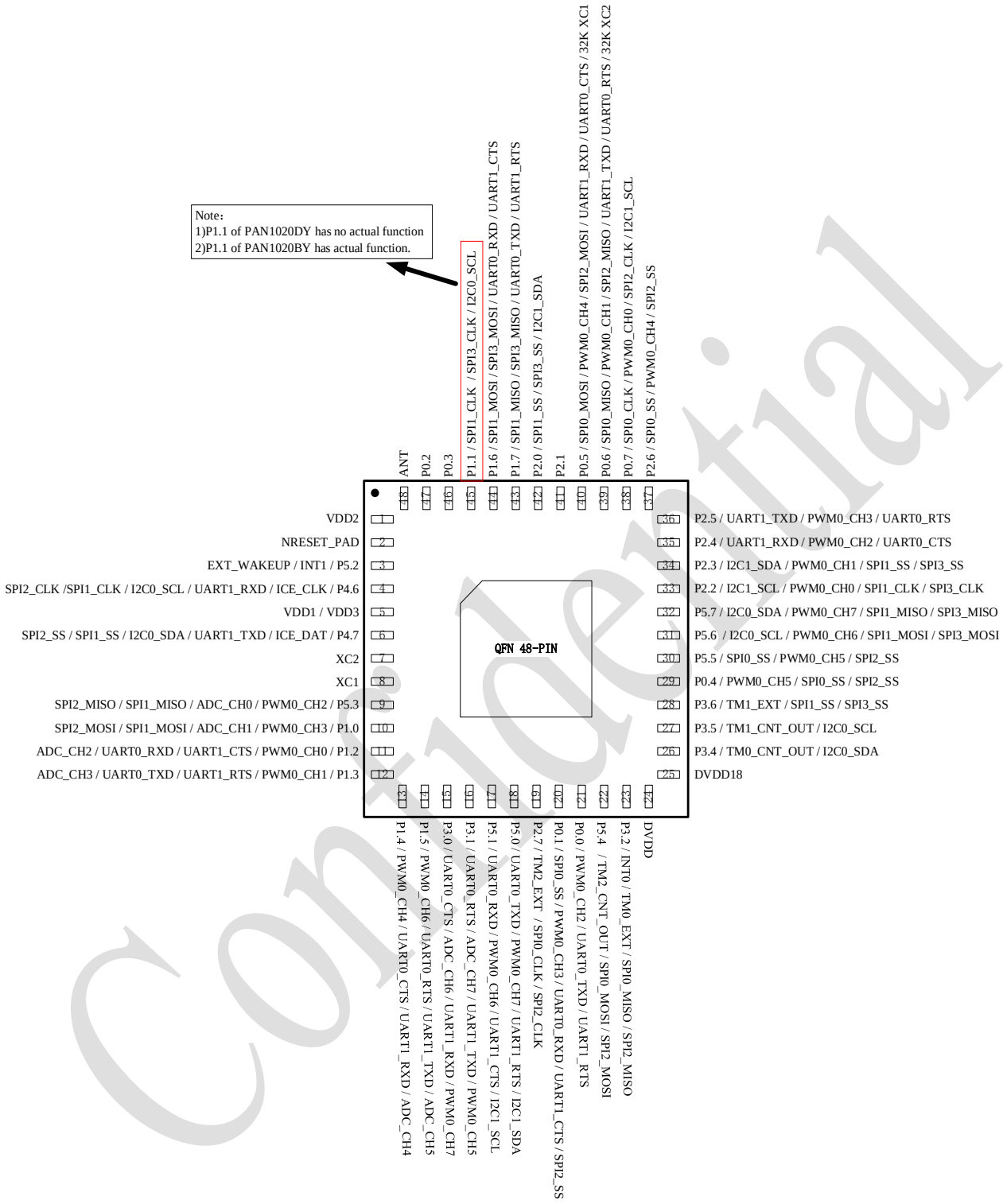


Figure 3-2 PAN1020 QFN 48-PIN Diagram

3.3 SSOP24-PIN Diagram

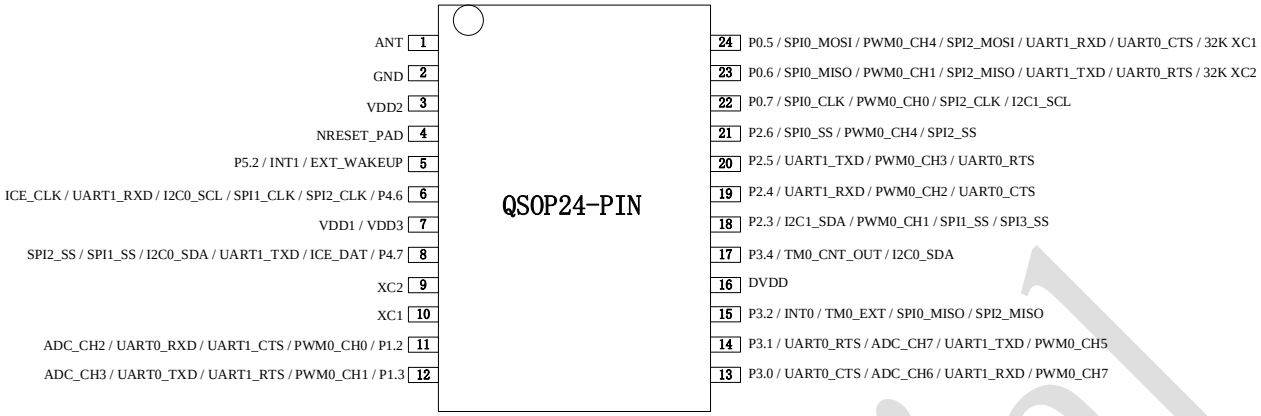


Figure 3-3 PAN1020 SSOP24-PIN Diagram

3.4 Pin Descriptions

Detail pin descriptions see Table 3-1.

Table 3-1 PAN1020 Pin descriptions

Pin Number			Pin Name	Pin Type	Description
QFN 32	QFN 48	SSOP24			
1	2	4	NRESET_PAD	I	Reset pin
2	3	5	P5.2	I/O	General purpose digital I/O pin
			INT1	I	External interrupt pin
			EXT_WAKEUP	I	External wake-up pin
3	4	6	P4.6	I/O	General purpose digital I/O pin
			ICE_CLK	I	ICE clk input pin
			UART1_RXD	I	UART1 RX pin
			I2C0_SCL	I/O	I2C0 CLK pin
			SPI1_CLK	O	SPI1 CLK pin
			SPI2_CLK	I	SPI2 CLK pin
4	5	7	VDD1	P	SoC power supply VDD1 pin
			VDD3	P	SoC power supply VDD3 pin
5	6	8	P4.7	I/O	General purpose digital I/O pin
			ICE_DAT	I	Debug and program data pin
			UART1_TXD	O	UART1 TX pin
			I2C0_SDA	I/O	I2C0 data pin

			SPI1_SS	O	SPI1 SS pin
			SPI2_SS	I	SPI2 SS pin
6	7	9	XC2	AO	Crystal pin2
7	8	10	XC1	AI	Crystal pin1
8	9	-	P5.3	I/O	General purpose digital I/O pin
			PWM0_CH2	O	PWM0 channel2 output pin
			ADC_CH0	AI	ADC channel0 analog input pin
			SPI1_MISO	I	SPI1 MISO pin
			SPI2_MISO	O	SPI2 MISO pin
9	10	-	P1.0	I/O	General purpose digital I/O pin
			PWM0_CH3	O	PWM0 channel3 output pin
			ADC_CH1	AI	ADC channel1 analog input pin
			SPI1_MOSI	O	SPI1 MOSI pin
			SPI2_MOSI	I	SPI2 MOSI pin
10	11	11	P1.2	I/O	General purpose digital I/O pin
			PWM0_CH0	O	PWM0 channel0 output pin
			UART1_CTS	I	UART1 CTS pin
			UART0_RXD	I	UART0 RX pin
			ADC_CH2	AI	ADC channel2 analog input pin
11	12	12	P1.3	I/O	General purpose digital I/O pin
			PWM0_CH1	O	PWM0 channel1 output pin
			UART1_RTS	O	UART1 RTS pin
			UART0_TXD	O	UART0 TX pin
			ADC_CH3	AI	ADC channel3 analog input pin
12	13	-	P1.4	I/O	General purpose digital I/O pin
			PWM0_CH4	O	PWM0 channel4 output pin
			UART0_CTS	I	UART0 CTS pin
			UART1_RXD	I	UART1 RX pin
			ADC_CH4	AI	ADC channel4 analog input pin
13	14	-	P1.5	I/O	General purpose digital I/O pin
			PWM0_CH6	O	PWM0 channel6 output pin
			UART0_RTS	O	UART0 RTS pin
			UART1_TXD	O	UART1 TX pin
			ADC_CH5	AI	ADC channel5 analog input pin

14	15	13	P3.0	I/O	General purpose digital I/O pin
			UART0_CTS	I	UART0 CTS pin
			ADC_CH6	AI	ADC channel6 analog input pin
			UART1_RXD	I	UART1 RX pin
			PWM0_CH7	O	PWM0 channel7 output pin
15	16	14	P3.1	I/O	General purpose digital I/O pin
			UART0_RTS	O	UART0 RTS pin
			ADC_CH7	AI	ADC channel7 analog input pin
			UART1_TXD	O	UART1 TX pin
			PWM0_CH5	O	PWM0 channel5 output pin
-	17	-	P5.1	I/O	General purpose digital I/O pin
			PWM0_CH6	O	PWM0 channel output pin
			UART0_RXD	I	UART0 RX pin
			UART1_CTS	I	UART1 CTS pin
			I2C1_SCL	I/O	I2C1 CLK pin
-	18	-	P5.0	I/O	General purpose digital I/O pin
			UART0_TXD	O	UART0 RX pin
			PWM0_CH7	O	PWM0 channel7 output pin
			UART1_RTS	O	UART1 RTS pin
			I2C1_SDA	I/O	I2C1 data pin
-	19	-	P2.7	I/O	General purpose digital I/O pin
			TM2_EXT	I	Timer2 external input pin
			SPI0_CLK	O	SPI0 CLK pin
			SPI2_CLK	I	SPI2 CLK pin
-	20	-	P0.1	I/O	General purpose digital I/O pin
			SPI0_SS	O	SPI0 SS pin
			PWM0_CH3	O	PWM0 channel3 output pin
			UART0_RXD	I	UART0 RX pin
			UART1_CTS	I	UART1 CTS pin
			SPI2_SS	I	SPI2 SS pin
-	21	-	P0.0	I/O	General purpose digital I/O pin
			PWM0_CH2	O	PWM0 channel2 output pin
			UART0_TXD	O	UART0 TX pin
			UART1_RTS	O	UART1 RTS pin

-	22	-	P5.4	I/O	General purpose digital I/O pin
			TM2_CNT_OUT	O	TM2_CNT output pin
			SPI0_MOSI	O	SPI0 MOSI pin
			SPI2_MOSI	I	SPI2 MOSI pin
-	23	15	P3.2	I/O	General purpose digital I/O pin
			INT0	I/O	External interrupt0
			TM0_EXT	I	Timer0 external input pin
			SPI0_MISO	I	SPI0 MISO pin
			SPI2_MISO	O	SPI2 MISO pin
16	24	16	DVDD	P	Core power supply, generaged by internal LDO
-	25	-	DVDD18	P	-
-	26	17	P3.4	I/O	General purpose digital I/O pin
			TM0_CNT_OUT	O	TM0_CNT output pin
			I2C0_SDA	I/O	I2C0 data pin
-	27	-	P3.5	I/O	General purpose digital I/O pin
			TM1_CNT_OUT	O	TM1_CNT output pin
			I2C0_SCL	I/O	I2C0 CLK pin
17	28	-	P3.6	I/O	General purpose digital I/O pin
			TM1_EXT	I	Timer1 external input pin
			SPI1_SS	O	SPI1 SS pin
			SPI3_SS	I	SPI3 SS pin
18	29	-	P0.4	I/O	General purpose digital I/O pin
			PWM0_CH5	O	PWM0 channel5 output pin
			SPI0_SS	O	SPI0 SS pin
			SPI2_SS	I	SPI2 SS pin
-	30	-	P5.5	I/O	General purpose digital I/O pin
			SPI0_SS	O	SPI0 SS pin
			PWM0_CH5	O	PWM0 channel5 output pin
			SPI2_SS	I	SPI2 SS pin
-	31	-	P5.6	I/O	General purpose digital I/O pin
			I2C0_SCL	I/O	I2C0 CLK pin
			PWM0_CH6	O	PWM0 channel6 output pin
			SPI1_MOSI	O	SPI1 MOSI pin
			SPI3_MOSI	I	SPI3 MOSI pin

19	32	-	P5.7	I/O	General purpose digital I/O pin
			I2C0_SDA	I/O	I2C0 data pin
			PWM0_CH7	O	PWM0 channel7 output pin
			SPI1_MISO	I	SPI1 MISO pin
			SPI3_MISO	O	SPI3 MISO pin
20	33	-	P2.2	I/O	General purpose digital I/O pin
			I2C1_SCL	I/O	I2C1 CLK pin
			PWM0_CH0	O	PWM0 channel0 output pin
			SPI1_CLK	O	SPI1 CLK pin
			SPI3_CLK	I	SPI3 CLK pin
21	34	18	P2.3	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I2C1 data pin
			PWM0_CH1	O	PWM0 channel1 output pin
			SPI1_SS	O	SPI1 SS pin
			SPI3_SS	I	SPI3 SS pin
22	35	19	P2.4	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 RX pin
			PWM0_CH2	O	PWM0 channel2 output pin
			UART0_CTS	I	UART0 CTS pin
23	36	20	P2.5	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 TX pin
			PWM0_CH3	O	PWM0 channel3 output pin
			UART0_RTS	O	UART0 RTS pin
24	37	21	P2.6	I/O	General purpose digital I/O pin
			SPI0_SS	O	SPI0 SS pin
			PWM0_CH4	O	PWM0 channel4 output pin
			SPI2_SS	I	SPI2 SS pin
25	38	22	P0.7	I/O	General purpose digital I/O pin
			SPI0_CLK	O	SPI0 CLK pin
			PWM0_CH0	O	PWM0 channel0 output pin
			SPI2_CLK	I	SPI2 CLK pin
			I2C1_SCL	I/O	I2C1 CLK pin
26	39	23	P0.6	I/O	General purpose digital I/O pin
			SPI0_MISO	I	SPI0 MISO pin

			PWM0_CH1	O	PWM0 channel1 output pin
			SPI2_MISO	O	SPI2 MISO pin
			UART1_TXD	O	UART1 TX pin
			UART0_RTS	O	UART0 RTS pin
			32K XC2	AO	32K Crystal pin2
27	40	24	P0.5	I/O	General purpose digital I/O pin
			SPI0_MOSI	O	SPI0 MOSI pin
			PWM0_CH4	O	PWM0 channel4 output pin
			SPI2_MOSI	I	SPI2 MOSI pin
			UART1_RXD	I	UART1 RX pin
			UART0_CTS	I	UART0 CTS pin
			32K XC1	AI	32K Crystal pin1
-	41	-	P2.1	I/O	General purpose digital I/O pin
28	42	-	P2.0	I/O	General purpose digital I/O pin
			SPI1_SS	O	SPI1 SS pin
			SPI3_SS	I	SPI3 SS pin
			I2C1_SDA	I/O	I2C1 data pin
-	43	-	P1.7	I/O	General purpose digital I/O pin
			SPI1_MISO	I	SPI1 MISO pin
			SPI3_MISO	O	SPI3 MISO pin
			UART0_TXD	O	UART0 TX pin
			UART1_RTS	O	UART1 RTS pin
-	44	-	P1.6	I/O	General purpose digital I/O pin
			SPI1_MOSI	O	SPI1 MOSI pin
			SPI3_MOSI	I	SPI3 MOSI pin
			UART0_RXD	I	UART0 RX pin
			UART1_CTS	I	UART1 CTS pin
-	45[Note]	-	P1.1	I/O	General purpose digital I/O pin (PAN1020DY does not have this function.)
			SPI1_CLK	O	SPI1 CLK pin (PAN1020DY does not have this function.)
			SPI3_CLK	I	SPI3 CLK pin (PAN1020DY does not have this function.)

			I2C0_SCL	I/O	I2C0 CLK pin (PAN1020DY does not have this function.)
29	46	-	P0.3	I/O	General purpose digital I/O pin
30	47	-	P0.2	I/O	General purpose digital I/O pin
31	48	1	ANT	AIO	Antenna pin
32	1	3	VDD2	P	RF power supply VDD2 pin
33	49	2	GND	P	Ground pin

Note: P1.1 of PAN1020DY has no actual function, P1.1 of PAN1020BY has actual function.

4 Electrical Characteristics

All the parameters are accurate to the one decimal place.

4.1 Absolute Maximum Ratings

Table 4-1 Absolute maximum ratings

Symbol	Description	Parameter			Unit
		Min	Typ	Max	
VDD	VDD1/VDD2	-0.3	-	3.6	V
V_I	Input voltage	-0.3	-	VDD	V
V_O	Output voltage	VSS	-	VDD	V
T_{OP}	Operating Temperature	-40	-	85	℃
T_{STG}	Storage Temperature	-40	-	125	℃

Note: Exceeding one or more of the limiting values may cause permanent damage to PAN1020.

Caution: Electrostatic sensitive device, comply with protection rules when operating.

4.2 DC Electrical Characteristics

Table 4-2 Voltage and current

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VDD1/VDD2	Power Supply	2.2	3	3.6	V	TA=25℃
VSS	Ground	-	0	-	V	-
$I_{DP\_SLP\_PAD}$	Deep sleep current	1.5	2	2.5	uA	MCU power down, SRAM maintain, HCLK and 32K RC off, wake up by GPIO or RE-SET
$I_{DP\_SLP\_RC}$	Deep sleep current	2	3	5	uA	MCU power down, SRAM maintain, HCLK off, 32K RC on
$I_{TX,0dBm}$	Operating Current of TX mode	-	17	-	mA	0dBm output power
$I_{TX,8dBm}$	Operating Current of TX mode	-	31	-	mA	8dBm output power
$I_{TX,10dBm}$	Operating Current of TX mode	-	41	-	mA	10dBm output power
I_{RX}	Operating Current of RX mode	-	16	-	mA	Maximum LNA Gain
V_{OH}	Output high level voltage	VDD-0.3	-	VDD	V	-
V_{OL}	Output low level voltage	VSS	-	VSS+0.3	V	-
V_{IH}	Input high level voltage	2.0	3	3.6	V	-
V_{IL}	Input low level voltage	VSS	-	VSS+0.3	V	-

4.3 16 MHz Crystal Oscillator Characteristics

Table 4-3 16M RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{XTAL(16M)}$	Crystal oscillator frequency	-	-	16	-	MHz
ESR(16M)	Equivalent series resistance	-	-	-	80	Ω
$\Delta f_{XTAL(16M)}$	Crystal frequency tolerance	-	-20	-	20	ppm
$V_{CLK(EXT)(16M)}$	External clock voltage	-	0.1	0.8	-	V
$\varphi N_{(EXTERNAL)16M}$	Phase noise	f_C = 50 kHz in case of an external reference clock	-	-	-130	dBc/Hz

4.4 32 KHz Crystal Oscillator Characteristics

Table 4-4 32K RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CLK(EXT)(32K)}$	External clock voltage	peak-peak voltage of external clock at XTAL32Kp, pin XTAL32Km floating. note: XTAL32Kp is internally AC coupled	0.1	0.2	1.5	V
$f_{XTAL(32k)}$	Crystal oscillator frequency	frequency range for an external clock (for a crystal, use either 32.000 kHz or 32.768 kHz)	TBD	32.768	TBD	KHz
ESR(32k)	Equivalent series resistance	-	-	-	100	KΩ
$\Delta f_{XTAL(32k)}$	Crystal frequency tolerance (including aging)	Timing accuracy is dominated by crystal accuracy. A much smaller value is preferred	-250	-	250	ppm

4.5 Digital Input/Output Characteristics

Table 4-5 Digital Input/Output Characteristics

Symbol	Paramter	Conditions	Min	Type	Max	Unit
RSTN pin						
V_{IH}	HIGH level input voltage	2.2≤VDD<3.6	0.4×VDD	-	VDD	V
V_{IL}	LOW level input voltage	2.2≤VDD<3.6	0	-	0.35×VDD	V
V_{hys}	Hysteresis voltage	2.2≤VDD<3.6	0.05×VDD	-	-	V
Standard I/O pins						
Input characteristics						
V_{IH}	HIGH level input voltage	2.2≤VDD<3.6	0.6× VDD	-	VDD	V
V_{IL}	LOW level input voltage	2.2≤VDD<3.6	0	-	0.4×VDD	V

V_{hys}	Hysteresis voltage	2.2≤VDD<3.6	0.05×VDD	-	-	V
Output characteristics						
V_O	Output voltage	Output active	0	-	VDD	V
V_{OH}	HIGH level output voltage	2.2≤VDD<3.6	VDD	-	-	V
V_{OL}	LOW level output voltage	2.2≤VDD<3.6	-	-	0	V
I_{OH}	HIGH level output current	VDD=3.3	-	20	-	mA
I_{OL}	LOW level output current	VDD=3.3	-	35	-	mA
R_{PD}	Pull down resistor	2.2≤VDD<3.6	-	50	-	kΩ

4.6 Stable Low Frequency RCX Oscillator Characteristics

Table 4-6 Stable Low Frequency RCX Oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{RC(RCX)}$	RCX oscillator frequency	default setting	-	32	-	Khz
$\Delta f_{RC(RCX)}$	RCX oscillator frequency drift	-	-500	-	500	ppm

4.7 AC Electrical Characteristics

Table 4-7 RF

Symbol	Condition	Min	Typ	Max	Unit
General frequency					
Fop	Operating frequency	2400	-	2483	MHz
PLL_{res}	PLL Programming resolution	-	1	-	MHz
Fxtal	Crystal frequency	-	16	-	MHz
DR	Data rate	-	1	-	Mbps
Transmitter					
PRF	Output power	2	8	13	dBm
PRFC	Output Power Range	-16	-	13	dBm
PBW	20dB Bandwidth for Modulated Carrier at 1Mbps	950	-	1100	MHz
Spur2M	In-band 2M Spurious Emission	-	-	-26	dBm
Spur≥3M	In-band 3M or greater Spurious Emission	-	-	-36	dBm
MDR	Maximum drift rate	-	-	13	KHz/50us
FD	Frequency Deviation	225	-	275	KHz
Receiver					
RXmax	Maximum received signal at <0.1% BER	-	0	-	dBm
RXSENS	Sensitivity (0.1%BER) @1Mbps	-	-90	-	dBm
C/ICO	C/I Co-channel interference	-	11	-	dBc
C/I1M	Adjacent 1MHz interference	-	-2	-	dBc
C/I2M	Adjacent 2MHz interference	-	-22	-	dBc
C/I≥3M	Adjacent ≥ 3MHz interference	-	-38	-	dBc
C/Iimage	Image frequency interference	-	-12	-	dBc

C/Iimage±1M	Adjacent（1MHz）interference to in-band image frequency	-	-35	-	dBc
P_IMD	Intermodulation interference	-	-45	-	dBm
P_Blocking	Out-of-band Blocking interference	-30		-	dBm

Table 4-8 DPLL

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD2	Power Supply	2.2	-	3.6	V	-
T_A	Temperature	-40	-	85	℃	-
Fin	Input Clock frequency	-	12	-	MHz	-
		-	16	-	MHz	-
		-	24	-	MHz	-
F_{DPLL}	Clock frequency	-	52	-	MHz	-

Table 4-9 ADC

Symbol	Parameter	Min	Typ	Max	Unit	Notes
-	Resolution	-	12	-	Bit	-
-	Significant Bits		10		Bit	
VDD2	Power Supply	2.5(for VTOP=2.4V) 2.2(for VTOP=1.4V)	-	3.6	VDDA	-
I_{TOT}	Operation Current	880	-	1600	uA	-
INL	Integral Nonlinearity Error	-	-	±2	LSB	
PCLK	System Clock	13	-	52	MHz	-
FS	Sample Rate	-	-	PCLK/30	MHz	-
Ts	Sample Time	2	-	128	PCLK	-
Th	Compare Time	24	-	96	PCLK	-
TCONV	Data Output cycle	30	50	234	PCLK	-
N	S-H counter	1	2	7	-	-
Vin	Analog input voltage	0.4 0.4	- -	2.4 1.4	V	-
Cin	Input Capacitance	-	10	-	pF	-
Rin	Input resistance	0.66	10	100	KΩ	See Note
Vref	ADC reference voltage	-	VBG（1.2V）	-	V	-
DATA	ADC Output	000	-	FFF	HEX	-
SFDR	Spurious Free Dynamic	-	64	-	dB	-

	range					

Note:

Sample time formula:

$$Ts= (EXTSMPT+1) *(ADCDIV +1)*T0$$

Continuous mode period formula:

$$T=(EXTSMPT+14) *(ADCDIV +1)* T0+2T0$$

T0: System clock, the maximum to 1/52M, or chosen as 1/26M, 1/13M.

Maximum resistance formula:

$$Rin < \frac{Ts}{Csample \ x \ ln(2^{N+1})} - R_{adc}$$

Ts: Sample Time, see the Table 4-9 for specific ranges. It is required to be stable within the DAC establishment period.

Csample: Sample capacitance =10pF

N: ADC bit defaults as 12. If the accuracy requirement is not high, it can be taken as 11,10,9,8, which can reduce the requirement of input impedance.

Radc: Sample switch resistance, 100Ω~300Ω

Table 4-10 Rin Maximum under Different Conditions

ADC significant bit	PCLK(Mhz)	Ts(cycles)	Ts(us)	Rinmax(KΩ)
12	26	2	0.08	0.753
12	26	8	0.31	3.314
12	26	32	1.23	13.558
12	26	64	2.46	27.217
12	26	128	4.92	54.534
12	13	2	0.15	1.607
12	13	8	0.62	6.729
12	13	32	2.46	27.217
12	13	64	4.92	54.534
12	13	128	9.85	109.169
9	13	2	0.15	2.119
9	13	8	0.62	8.778
9	13	32	2.46	35.412
9	13	64	4.92	70.924
9	13	128	9.85	141.949
9	13	2	0.08	1.009

9	13	8	0.31	4.339
9	13	32	1.23	17.656
9	13	64	2.46	35.412
9	13	128	4.92	70.924

Table 4-11 LVR

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD2	Power Supply	2.2	3	3.6	V	-
V_{LVR}	Threshold Voltage	1.6	1.7	1.8	V	-

Table 4-12 BOD

Symbol	Parameter	Vout(V) 1→0	Vout(V) 0→1	Test Conditions	Notes
V_{BOD}	Brown-Out Detector	1.93	2.06	BODEN=1 BODVL<1:0>=00	-
		2.20	2.34	BODEN=1 BODVL<1:0>=01	-
		2.55	2.72	BODEN=1 BODVL<1:0>=10	-
		2.82	2.87	BODEN=1 BODVL<1:0>=11	-

5 Application Reference Design

5.1 QFN-32 Application Reference Circuit

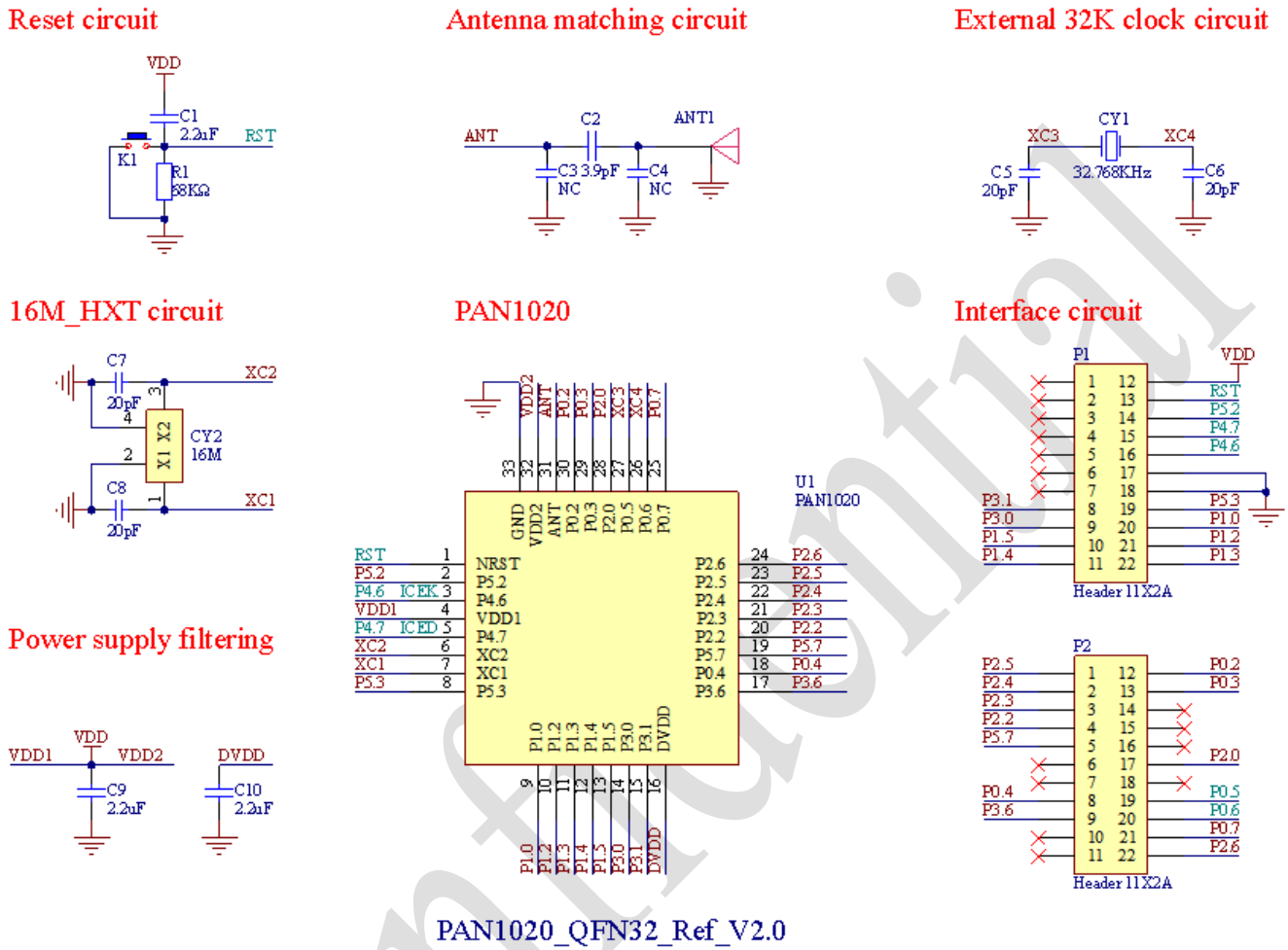


Figure 5-1 Application Reference Circuit for QFN32

5.2 QFN-48 Application Reference Circuit

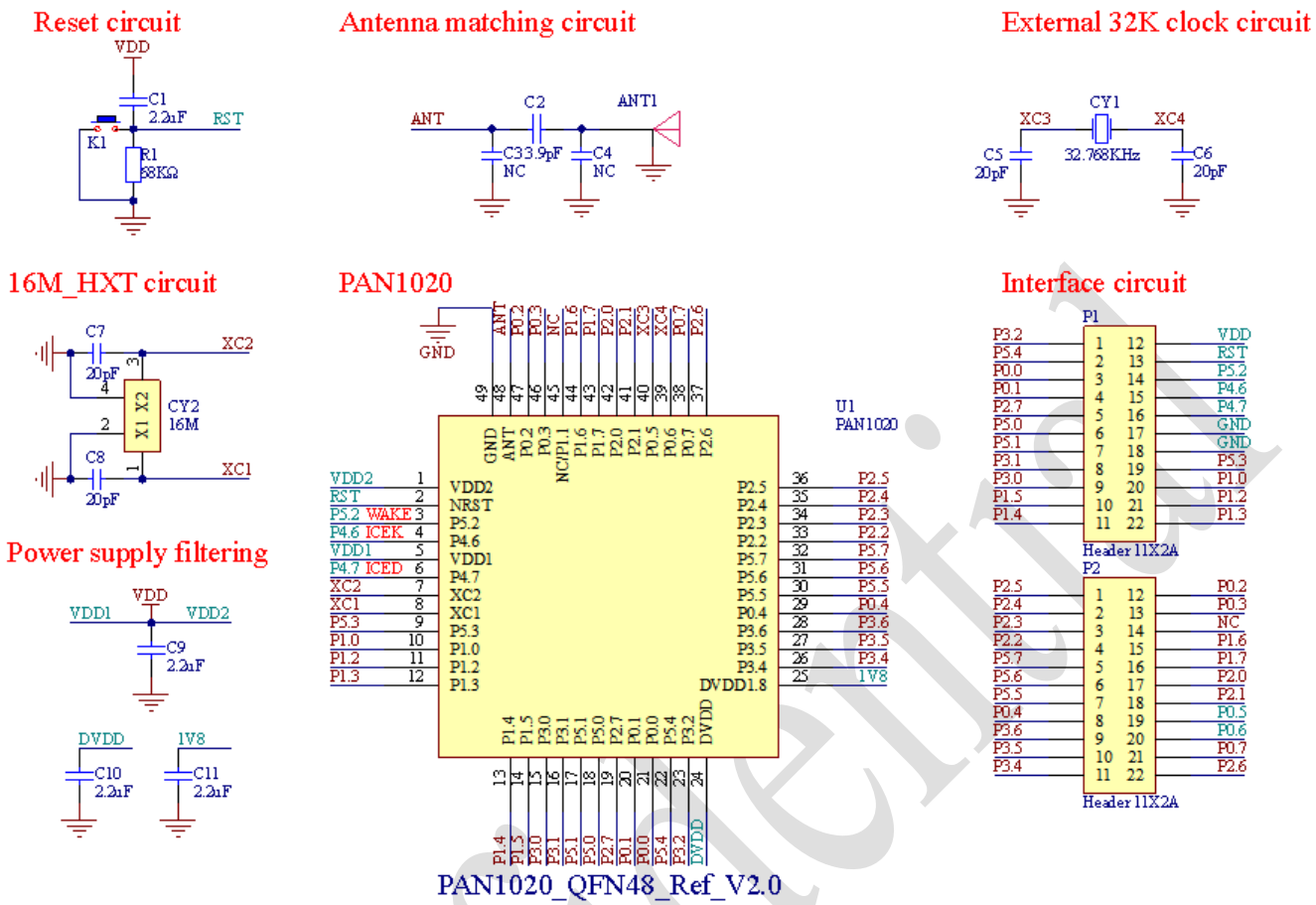


Figure 5-2 Application Reference Circuit for QFN48

Note: P1.1 of PAN1020DY has no actual function, P1.1 of PAN1020BY has actual function.

5.3 SSOP24 Application Reference Circuit

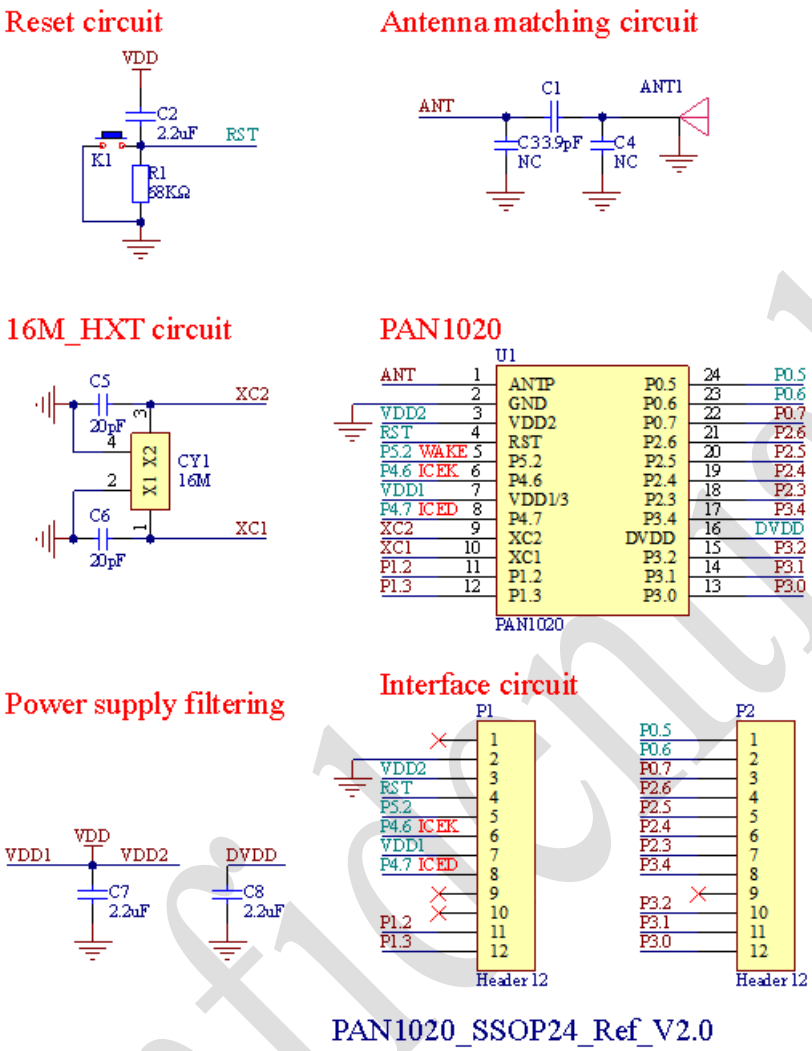


Figure 5-3 Application Reference Circuit for SSOP24

6 Pakage Dimensions

6.1 QFN-32 Package Dimensions

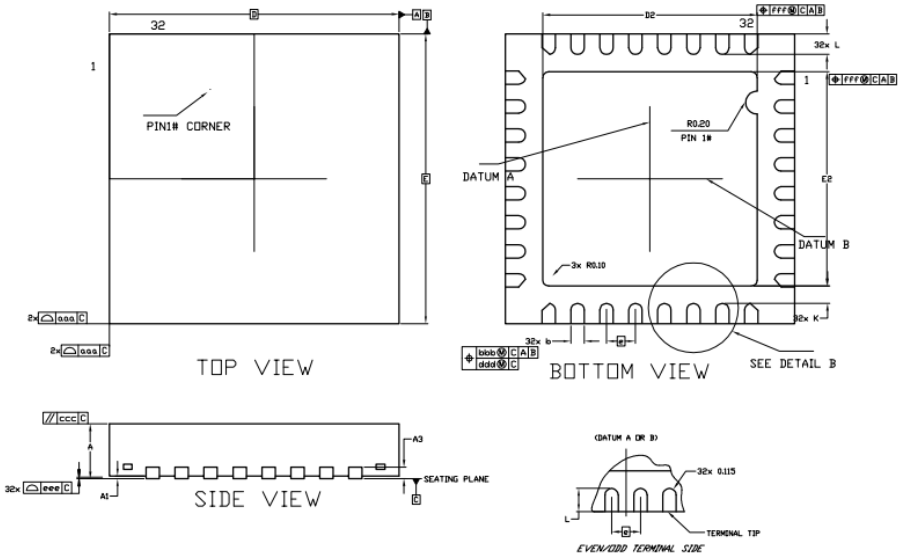


Figure 6-1 QFN32 Package Views

Table 6-1 QFN32 Package Detail Parameters

DIM / SYMBOL	MIN.(mm)	NOM.(mm)	MAX.(mm)
A	0.70	0.75	0.80
	0.85	0.90	0.95
A1	0	0.02	0.05
A3	-	0.20 REF	-
b	0.18	0.23	0.28
D	5.00BSC		
E	5.00BSC		
D2	3.55	3.65	3.75
E2	3.55	3.65	3.75
e	0.50BSC		
L	0.30	0.35	0.40
K	0.20	-	-
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

6.2 QFN-48 Package Dimensions

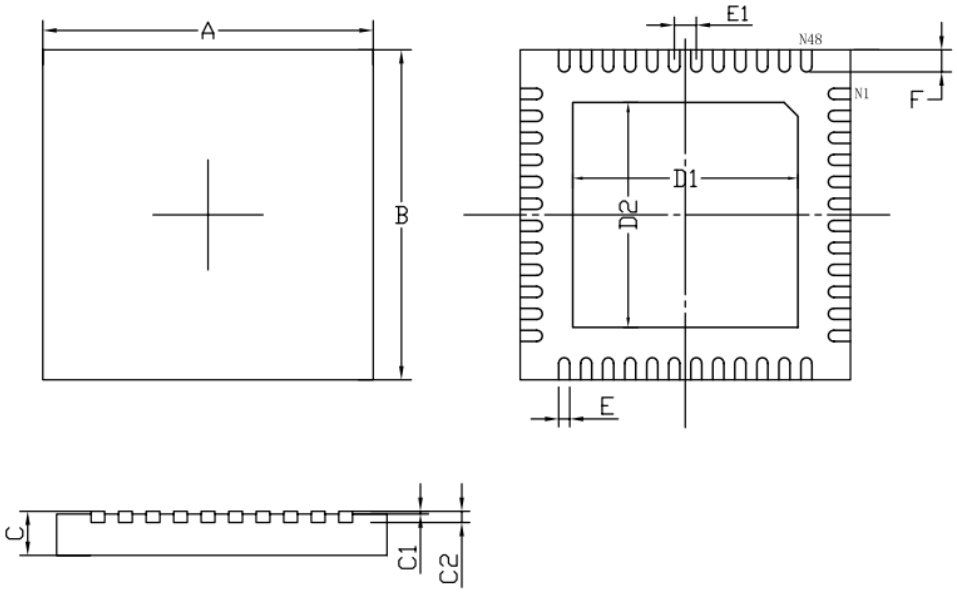


Figure 6-2 QFN48 Package Views

Table 6-2 QFN48 Package Detail Parameters

DIM / SYMBOL	MIN.(mm)	MAX.(mm)
A	6.0±0.1	
B	6.0±0.1	
C	0.70	0.80
C1	0~0.050	
C2	0.203TYP	
D1	4.05TYP	
D2	4.05TYP	
E	0.200TYP	
E1	0.400TYP	
F	0.400TYP	

6.3 SSOP24 Package Dimensions

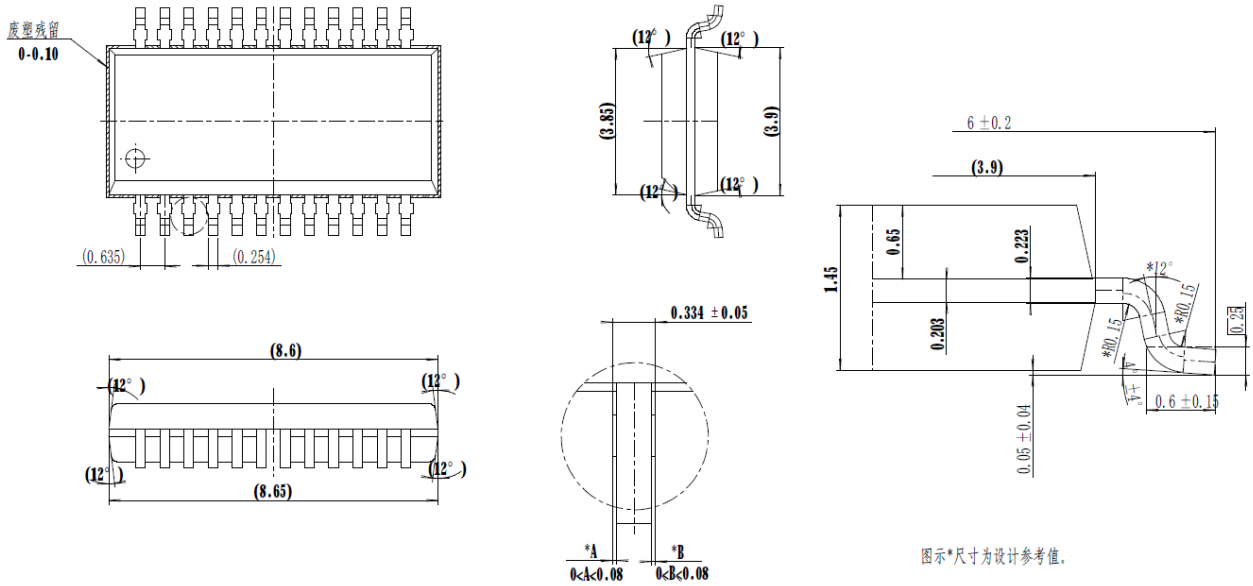


Figure 6-3 SSOP24 Package Views

7 Precautions

1) This product is a CMOS device and should be protected against static electricity during storage, transportation and use.
2) Grounding when device is in use.
3) Reflow temperature can not exceed 260℃.

8 Storage Conditions

1) Products should be stored in sealed packages: when the temperature is less than 30 degrees and the humidity is less than 90%, it can last for 12 months.
2) After the package is opened, the components will be used in the reflow process or other high-temperature processes. The following conditions must be met:
   a) Completed within 72 hours and the factory environment is less than 30℃≤ 60% RH.
   b) Stored in 10% RH environment.
   c) Exhaust at 125℃ for 24 hours to remove internal water vapor before used.