PANCHIP

PAN3730 series

Datasheet

V1.0 Feb. 2023

Panchip Microelectronics Co., Ltd.

Sub-1G & 2.4G SoC Transceiver

General Description

The PAN3730 series is an SOC chip that integrates a dual-band transceiver with Sub-1G and 2.4G.
The Sub-1G band is a low-power long-range wireless transceiver chip using ChirpIoT™ modulation and demodulation technology. It supports half-duplex wireless communication. The operating frequency band is 370~590MHz and 740~1180MHz. The chip has the characteristics such as high anti-interference, high sensitivity, low power consumption and ultra-long transmission range. The industry-leading link budget, along with the -140dBm sensitivity and the 22dBm maximum output power makes this chip the best choise for long-range transmission and extremely high reliability applications.
Compared with conventional modulation techniques, PAN3730 also has significant advantages in blocking and adjacent channel selection, which further improves communication reliability. A lot of chip parameters, such as bandwidth, spreading factor, coding rate of forward error correction, can be configured for trade-off among distance, anti-interference ability and power consumption, which ensures sufficient flexibility.
The 2.4G band supports BLE5.3 and 2.4GHz dual-mode operating modes, which works in the 2.400-2.483GHz universal ISM frequency band. There is an external 1MB Flash program memory and a built-in 64KB SRAM memory. In addition, PAN3730 series is equipped with a wealth of peripherals, including up to 30 GPIOs, 24-channel PWM, three 32-bit timers, 1 I2C, 2 UARTs, 2 SPIs, 8 external channels ADC, WDT, WWDT, I2S master, I2S slave, USB2.0(Full Speed), 32K RC automatic calibration, QDEC and automatic key-scan, etc.

Key Features

Sub-1G

- Frequency band: 370~590 MHz, 740~1180MHz
- Modulation: ChirpIoT™
- Transmitter output power: -7dBm ~ 22dBm
- Max link budget: 162dB
- Sensitivity: -140dBm@62.5kHz
- Operating current
  - Deep Sleep mode current:400nA
  - Receiving current: 12.5mA@DCDC mode
  - Transmitting current: 135mA@22dBm, 83mA@18dBm, 25mA@0dBm
- Bandwidth: 62.5kHz, 125kHz, 250kHz, 500kHz
- Spreading Factor (SF): 7~12, supports automatic identification of spread factors
- Coding Rate (CR): 4/5, 4/6, 4/7, 4/8
- Supports CAD function
- Data rate: 0.08~20.4Kbps
- Supports 4-wire SPI configuration interface and 2 GPIOs
- Fully integrated frequency synthesizer

2.4G

- **RF**
  - Frequency band: 2.400 ~ 2.483 GHz
  - Mode
  - BLE5.3 modes:
    1Mbps, 2Mbps, 500kbps, 125kbps
  - 2.4G private protocol:
    1Mbps / 2Mbps, supporting hardware ACK
  - Output power: -45dBm~7dBm
  - Receiver
    - -100dBm@125kbps
    - -99dBm@500kbps
    - -96dBm@1Mbps
    - -93dBm@2Mbps
  - RSSI
    - Resolution: 0.25dB
    - Accuracy: ±2dB
    - Range: - 90dbm ~ -15dBm
  - Positioning: AoA/AoD supported
  - Single antenna supported
  - Safety regulations: BQB / ETSI / FCC
- **MCU**
  - 32-bit MCU core running up to 64MHz
- **Memory**
  - Build-in 1MB flash supporting deep sleep mode
  - 64KB SRAM
  - 256B eFuse
  - 4 KB cache
- **Low Power**
  - Active mode RX: 5.6mA(DCDC)
  - Active mode TX at 0dBm: 6.1mA(DCDC)
  - Standby mode: 0.34uA
  - Standby mode(SRAM retention): 2uA(GPIO, XTL, RCL can wake up)
  - Deep sleep mode: 8uA(All Logic Retention, GPIO, XTL, RCL can wake up)
- **Clock**
  - 32MHz RC
  - 32MHz XTAL
  - 32kHz RC
  - 32.768kHz XTAL
  - DPLL
    2 channels: 64MHz/48MHz and 48MHz(USB 2.0)

- **Peripheral**
  - Up to 30 GPIOs (there are two power supply voltages)
  - 24-channel PWM
  - Three 32-bit timer
  - One I2C
  - Two UARTs
  - Two SPIs
  - DMA
  - 11-channel ADC(8 ext, bandgap, VDD/4, temp)
  - Two I2S(one I2S master and one I2S slave)
  - 3-channel QDEC
  - WDT / WWDT
  - ECC accelerator
  - Automatic key-scan
  - IO / BOD / POR / LVR / System reset
  - FMC(Support IAP, support the boot loader with address 0x0)
  - Clock measurement and clock calibration
  - USB2.0(Full_speed)
  - Flash data encryption
- **Temperature Sensor**
  - Support temperature sensor
  - Test range: -40℃ ~ 85℃
  - Accuracy: ±2℃ (With calibration)
- **Package**
  - QFN64
- **Operating Condition**
  - Operating temperature: -40℃ ~ 85℃
  - Operating voltage: 2V ~ 3.6V（DCDC）

Typical Applications

- Smart Firefighting
- Smart Healthcare
- Smart Meter
- Smart Location System
- Smart Security
- Smart Sensor

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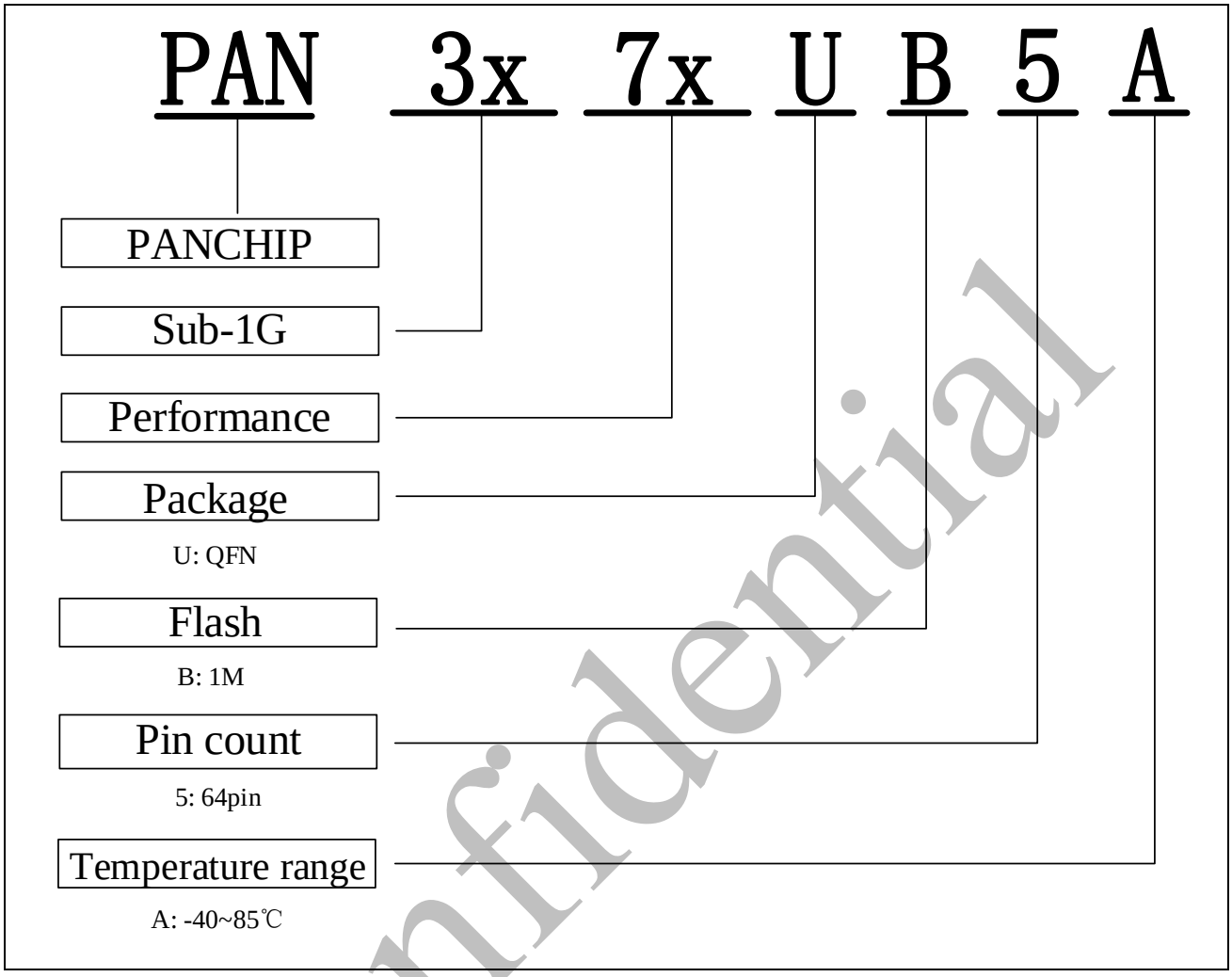
1 Naming rule



2 Order information

Part number	Type	Package	Pin count	IO	FLASH	RAM	Temperature range	Packing
PAN3730UB5A	Sub-1G	QFN	64	30	1M	64K	-40~85℃	Tape & Reel

Before ordering, please contact the sales window for the latest mass production information.

3 Block Diagram

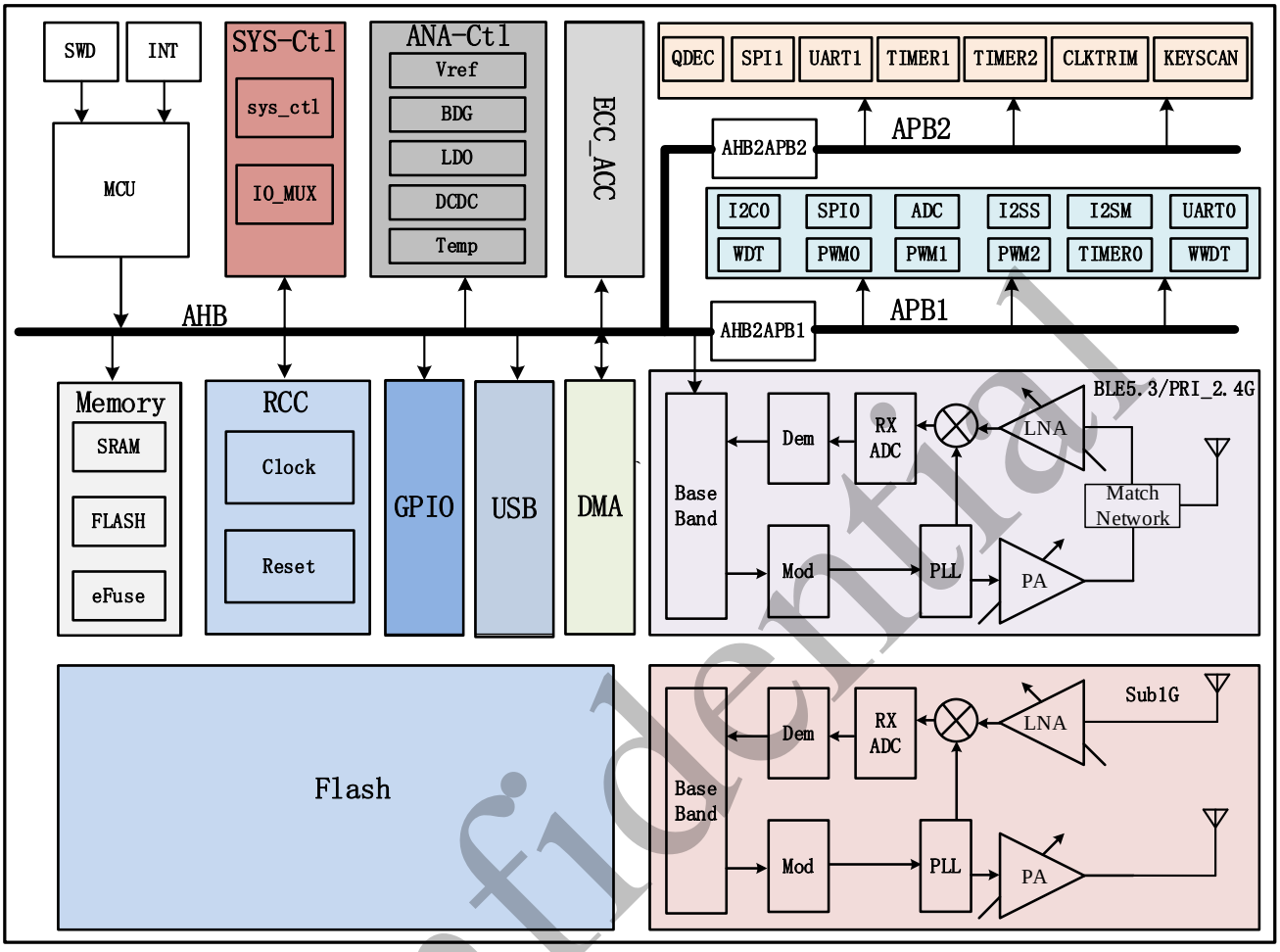


Figure 3-1 Block Diagram

4 Pin Information

4.1 Pin Diagram

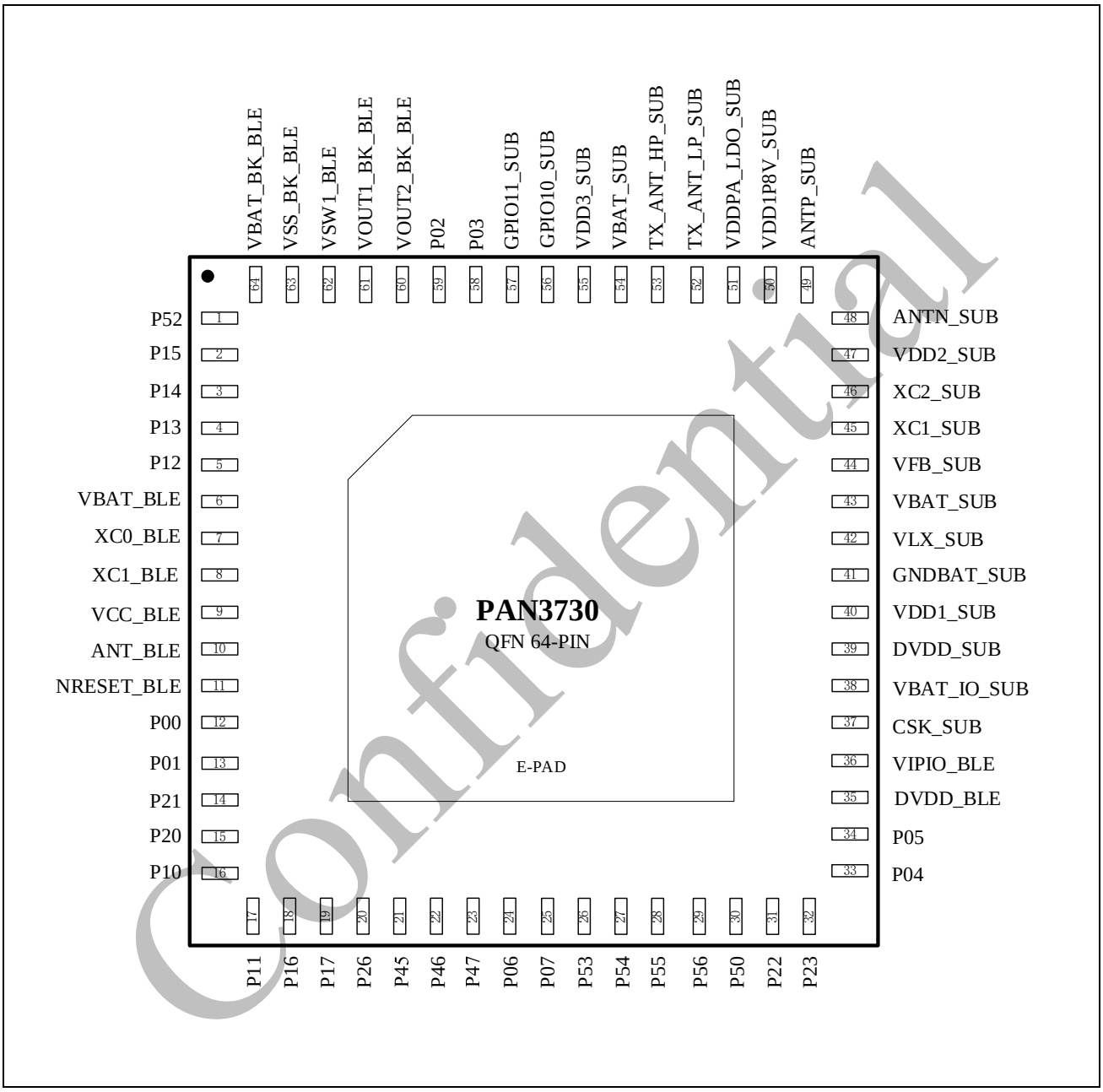


Figure 4-1 QFN64 Diagram

4.2 Pin Descriptions

Table 4-1 Pin Descriptions

Pin No.	Pin Name	Pin Type	Description
1	P52	I/O	General-purpose digital input and output pin
	ADC_TRG	I	Adc external trg input pin
	SPI1_CS	I/O	Spi1 chip select pin
	ADC_CH3	AI	Adc channel 3 pin
	KS_O2	O	Keyscan output channel 2 pin
	ANT_SW7	O	Antenna switch 7 pin
2	P15	I/O	General-purpose digital input and output pin
	UART1_RX	I	Uart1 rx pin
	ANT_SW7	O	Antenna switch 7 pin
	I2C0_SCL	I/O	I2c0 scl pin
	PWM0_CH5	O	Pwm0 channel 5 output pin
	KS_I5	I	Keyscan input channel 5 pin
	QDEC_X1	I	Qdec x input channel 1 pin
3	P14	I/O	General-purpose digital input and output pin
	UART1_TX	O	Uart1 tx pin
	I2C0_SDA	I/O	I2c0 sda pin
	ANT_SW6	O	Antenna switch 6 pin
	PWM0_CH4	O	Pwm0 channel 4 output pin
	KS_I4	I	Keyscan input channel 4 pin
	QDEC_X0	I	Qdec x input channel 0 pin
4	P13	I/O	General-purpose digital input and output pin
	I2C0_SDA	I/O	I2c0 sda pin
	I2S_S_WS	I	I2s slave chip select input pin
	I2S_M_WS	O	I2s master chip select output pin
	PWM0_CH7	O	Pwm0 channel 7 output pin
	ANT_SW4	O	Antenna switch 4 pin
	XL1	AO	External 32.768kHz clock source output
5	P12	I/O	General-purpose digital input and output pin
	I2C0_SCL	I/O	I2c0 clk pin
	I2S_S_CLK	I	I2s slave clock input pin

Pin No.	Pin Name	Pin Type	Description
	I2S_M_CLK	O	I2s master clock output pin
	PWM0_CH6	O	Pwm0 channel 6 output pin
	XL0	AI	External 32.768kHz clock source input
6	VBAT_BLE	P	The power input pin of the chip
7	XC0_BLE	AI	External 32MHz clock source input
8	XC1_BLE	AO	External 32MHz clock source output
9	VCC_BLE	P	Power supply port
10	ANT_BLE	AI/AO	RF antenna pin, an external antenna is required for use
11	NRESET_BLE	I	Reset pin
12	P00	I/O	General-purpose digital input and output pin
	UART0_TX	O	Uart0 tx pin
	I2C0_SCL	I/O	I2c0 clock pin
	TIMER0_OUT	O	Timer0 output pin
	PWM0_CH0	O	Pwm0 channel 0 output pin
	I2S_M_SDI	I	I2s master data input pin
	KS_O6	O	Keyscan output channel 6 pin
	I2S_S_SDI	I	I2s slave data input pin
13	P01	I/O	General-purpose digital input and output pin
	UART0_RX	I	Uart0 rx pin
	I2C0_SDA	I/O	I2c0 data pin
	I2S_M_SDO	O	I2s master data output pin
	PWM0_CH1	O	Pwm0 channel 1 output pin
	I2S_S_SDO	O	I2s slave data output pin
	KS_O7	O	Keyscan output channel 7 pin
14	P21	I/O	General-purpose digital input and output pin
	SPI1_CLK	I/O	Spi1 clock pin
	TIMER2_EXT	I	Timer2 external input pin
	ADC_CH7	AI	Adc channel 7 pin
	KS_I1	I	Keyscan input channel 1 pin
	QDEC_Z1	I	Qdec z input channel 1 pin
15	P20	I/O	General-purpose digital input and output pin
	SPI1_CS	I/O	Spi1 cs pin
	TIMER1_EXT	I	Timer1 input pin

Pin No.	Pin Name	Pin Type	Description
	ADC_CH6	AI	Adc channel 6 pin
	KS_I0	I	Keyscan input channel 0 pin
	QDEC_Z0	I	Qdec z input channel 0 pin
16	P10	I/O	General-purpose digital input and output pin
	SPI0_MOSI	I/O	Spi0 mosi pin
	TIMER0_EXT	I	Timer0 external input pin
	ADC_CH5	AI	Adc channel 5 pin
	PWM0_CH4	O	Pwm0 channel 4 output pin
	KS_O4	O	Keyscan output channel 4 pin
17	P11	I/O	General-purpose digital input and output pin
	SPI0_MISO	I/O	Spi0 miso pin
	CLKTRIM_EXT	I	CLKTRIM external clock measurement input pin
	ADC_CH4	AI	Adc channel 4 pin
	PWM0_CH5	O	Pwm0 channel 5 output pin
	KS_O5	O	Keyscan output channel 5 pin
	I2S_MCLK	O	I2s output sample clock
18	P16	I/O	General-purpose digital input and output pin
	UART1_CTS	I	Uart1 cts pin
	ANT_SW4	O	Antenna switch 4 pin
	TIMER0_OUT	O	Timer0 output pin
	PWM0_CH6	O	Pwm0 channel 6 output pin
	KS_I6	I	Keyscan input channel 6 pin
	QDEC_Y0	I	Qdec y input channel 0 pin
19	P17	I/O	General-purpose digital input and output pin
	UART1_RTS	O	Uart1 rts pin
	TIMER1_OUT	O	Timer1 output pin
	PWM0_CH7	O	Pwm0 channel 7 output pin
	KS_I7	I	Keyscan input channel 7 pin
	QDEC_Y1	I	Qdec y input channel 1 pin
20	P26	I/O	General-purpose digital input and output pin
	UART1_CTS	I	Uart1 cts pin
	UART0_TX	O	Uart0 tx pin
	SPI1_MISO	I/O	Spi1 miso pin

Pin No.	Pin Name	Pin Type	Description
	KS_O14	O	Keyscan output channel 14 pin
	PWM1_CH2	O	Pwm1 channel 2 output pin
21	P45	I/O	General-purpose digital input and output pin
	PWM2_CH0	O	Pwm2 channel 0 output pin
	KS_O22	O	Keyscan output channel 22 pin
22	P46	I/O	General-purpose digital input and output pin
	SWD_CLK	I	Swd clock input pin
	UART1_RX	I	Uart1 rx pin
	I2C0_SCL	I/O	I2c0 scl pin
	SPI0_CLK	I/O	Spi0 clock pin
	ANT_SW5	O	Antenna switch 5 pin
	KS_O0	O	Keyscan output channel 0 pin
23	P47	I/O	General-purpose digital input and output pin
	SWD_DAT	I/O	Swd data input output pin
	UART1_TX	O	Uart1 tx pin
	I2C0_SDA	I/O	I2c0 sda pin
	SPI0_CS	I/O	Spi0 cs pin
	ANT_SW6	O	Antenna switch 6 pin
	KS_O1	O	Keyscan output channel 1 pin
24	P06	I/O	General-purpose digital input and output pin
	SPI1_CS	I/O	Spi1 cs pin
	UART1_TX	O	Uart1 tx pin
	ANT_SW3	O	Antenna switch 3 pin
	PWM1_CH2	O	Pwm1 channel 2 output pin
	KS_O12	O	Keyscan output channel 12 pin
	QDEC_Y0	I	Qdec y input channel 0 pin
	I2S_MCLK	O	I2s output sample clock
25	P07	I/O	General-purpose digital input and output pin
	SPI1_CLK	I/O	Spi1 clock pin
	UART1_RX	I	Uart1 rx pin
	TIMER0_EXT	I	Timer0 external input pin
	PWM1_CH3	O	Pwm1 channel 3 output pin
	KS_O13	O	Keyscan output channel 13 pin

Pin No.	Pin Name	Pin Type	Description
	QDEC_Y1	I	Qdec y input channel 1 pin
	ANT_SW5	O	Antenna switch 5 pin
26	P53	I/O	General-purpose digital input and output pin
	PWM1_CH3	O	Pwm1 channel 3 output pin
	KS_O3	O	Keyscan output channel 3 pin
	QDEC_Y_IDX	I	Qdec y_idx input pin
27	P54	I/O	General-purpose digital input and output pin
	PWM2_CH2	O	Pwm2 channel 2 output pin
	KS_O23	O	Keyscan output channel 23 pin
	QDEC_Z_IDX	I	Qdec z_idx input pin
28	P55	I/O	General-purpose digital input and output pin
	PWM2_CH3	O	Pwm2 channel 3 output pin
	KS_O4	O	Keyscan output channel 4 pin
	QDEC_X0	I	Qdec x input channel 0 pin
29	P56	I/O	General-purpose digital input and output pin
	PWM1_CH6	O	Pwm1 channel 6 output pin
	UART0_CTS	I	Uart0 cts pin
	UART1_TX	O	Uart1 tx pin
	QDEC_X0	I	Qdec x input channel 0 pin
	KS_O11	O	Keyscan output channel 11 pin
30	P50	I/O	General-purpose digital input and output pin
	PWM2_CH1	O	Pwm2 channel 1 output pin
	KS_O0	O	Keyscan output channel 0 pin
31	P22	I/O	General-purpose digital input and output pin
	QDEC_X_IDX	I	Qdec x_idx input pin
	PWM1_CH4	O	Pwm1 channel 4 output pin
	I2S_S_CLK	I	I2s slave data input pin
	SPI1_MISO	I/O	Spi1 miso pin
	KS_I2	I	Keyscan input channel 2 pin
	I2S_M_CLK	O	I2s master clock output pin
32	P23	I/O	General-purpose digital input and output pin
	QDEC_Y_IDX	I	Qdec y_idx input pin
	PWM1_CH5	O	Pwm1 channel 5 output pin

Pin No.	Pin Name	Pin Type	Description
	I2S_S_WS	I	I2s slave chip select input pin
	SPI1_MOSI	I/O	Spi1 mosi pin
	KS_I3	I	Keyscan input channel 3 pin
	I2S_M_WS	O	I2s master chip select output pin
33	P04	I/O	General-purpose digital input and output pin
	I2S_S_SDI	I	I2s slave data input pin
	I2S_M_SDI	I	I2s master data input pin
	TIMER2_OUT	O	Timer2 output pin
	PWM1_CH0	O	Pwm1 channel 0 output pin
	KS_O10	O	Keyscan output channel 10 pin
	QDEC_X0	I	Qdec x input channel 0 pin
34	P05	I/O	General-purpose digital input and output pin
	I2S_S_SDO	O	I2s slave data output pin
	I2S_M_SDO	O	I2s master data output pin
	ANT_SW2	O	Antenna switch 2 pin
	PWM1_CH1	O	Pwm1 channel 1 output pin
	KS_O11	O	Keyscan output channel 11 pin
	QDEC_X1	I	Qdec x input channel 1 pin
	ADC_TRG	I	Adc external trg input pin
35	DVDD_BLE	P	Hldo output pin, typical value 1.2V
36	VIPIO_BLE	P	IO power supply pin
37	CSK_SUB	I/O	SPI clock, needs to be connected to SPI0 CLK (P03)
38	VBAT_IO_SUB	P	Digital GPIO power supply, connected to the main power supply
39	DVDD_SUB	P	Digital power LDO output
40	VDD1_SUB	P	Analog power supply, connected to VFB in DCDC mode, connected to the main power supply in non-DCDC mode
41	GNDBAT_SUB	P	Analog ground
42	VLX_SUB	AO	Internal DCDC output, connected to external series inductor in DCDC mode, NC in non-DCDC mode
43	VBAT_SUB	P	Analog power supply, connected to the main power supply
44	VFB_SUB	I	Internal DCDC feedback input, connected to VDD in DCDC mode, NC in non-DCDC mode
45	XC1_SUB	AI	Crystal oscillator input

Pin No.	Pin Name	Pin Type	Description
46	XC2_SUB	AO	Crystal oscillator output
47	VDD2_SUB	P	Analog power supply, connected to VFB in DCDC mode, connected to the main power supply in non-DCDC mode
48	ANTN_SUB	AI	Antenna Pin（Negative）
49	ANTP_SUB	AI	Antenna Pin（Positive）
50	VDD1P8V_SUB	P	Low power PA LDO power supply, connected to VFB in DCDC mode, connected to the main power supply in non-DCDC mode
51	VDDPA_LDO_SUB	P	Low power LDO output
52	TX_ANT_LP_SUB	AO	Transmitter low power PA output
53	TX_ANT_HP_SUB	AO	Transmitter high power PA output
54	VBAT_SUB	P	Analog power supply, connect to the main power supply
55	VDD3_SUB	P	Analog power supply, connected to VFB in DCDC mode, connected to the main power supply in non-DCDC mode
56	GPIO10_SUB	I	Digital input Pin
		O	External PA enable control signal
57	GPIO11_SUB	I	Digital input and output pin
		O	Channel status indication signal
58	P03	I/O	General-purpose digital input and output pin
	UART0_RTS	O	Uart0 rts pin
	ANT_SW1	O	Antenna switch 1 pin
	SPI0_CLK	I/O	Spi0 clock pin
	USB_DP	AI/AO	Usb dp pin
	PWM0_CH3	O	Pwm0 channel 3 output pin
	KS_I1	I	Keyscan input channel 1 pin
59	P02	I/O	General-purpose digital input and output pin
	UART0_CTS	I	Uart0 cts pin
	ANT_SW0	O	Antenna switch 0 pin
	SPI0_CS	I/O	Spi0 cs pin
	USB_DM	AI/AO	Usb dm pin
	PWM0_CH2	O	Pwm0 channel 2 output pin
	KS_I0	I	Keyscan input channel 0 pin
60	VOUT2_BK_BLE	P	DCDC-2 voltage output pin, power supply to internal Flash

Pin No.	Pin Name	Pin Type	Description
61	VOUT1_BK_BLE	P	DCDC-1 voltage output pin, can be directly connected to VCC_RF pin
62	VSW1_BLE	P	DCDC internal power switch (switching frequency is about 650kHz), an external inductor is required when using
63	VSS_BK_BLE	P	Common ground terminal of DCDC power supply, independent power ground
64	VBAT_BK_BLE	P	The power input pin of the chip
65	E-PAD	P	Chip bottom pad, common ground

4.3 Internal connection

Table 4-2 RF and MCU internal connection

Pin Status	RF	MCU
I S	PAD_MOSI_3V	P30
I S	PAD_MISO_3V	P31
I S	PAD_CSN_3V	P41
I S	PAD_IRQ_3V	P27

5 Electrical specification

Maximum and minimum values

In the notes below each table, the data obtained through comprehensive evaluation, design simulation and/or process features are not tested on the production line; based on the comprehensive evaluation, the minimum and maximum values are after the sample test. Take the average value and add and subtract three times the standard distribution (average ± 3 Σ).

5.1 Sub-1G

Note: The VDD and other parameters described in this section correspond to the power input pins such as "xxx_SUB" in the Pin Information.

5.1.1 Absolute maximum rating

Test Conditions:

- Supply voltage : 3.3V
- Temperature : 25℃

Table 5-1 Absolute maximum rating

Symbol	Description	Parameter			Unit
		Min	Min	Min	
VDD	Power supply voltage	-0.3	3.3	3.6	V
V_I	Input voltage	-0.3	-	VDD	V
V_O	Output voltage	VSS	-	VDD	V
T_{OP}	Operating temperature	-40	-	85	℃
T_{STG}	Storage temperature	-55	-	125	℃
T_J	Junction temperature	-	-	130	℃

Note:

- Exceeding one or more maximum ratings may cause permanent damage.
- Electrostatic sensitive equipment, operate in accordance with the protection rules.

5.1.2 Current Consumption

Test Conditions:

- Supply voltage: 3.3V
- Temperature: 25℃
- Frequency: 490MHz

Table 5-2 Voltage and Current

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
VDD	Power supply voltage	1.8	3.3	3.6	V	TA=25℃, non-DCDC mode
		2	3.3	3.6	V	TA=25℃, DCDC mode
VSS	Ground	-	0	-	V	-
$I_{DeepSleep}$	Deep sleep mode current	-	400	-	nA	-
$I_{TX,22dBm}$	Operating current in TX mode	-	135	-	mA	22dBm output power
$I_{TX,18dBm}$		-	83	-	mA	18dBm output power
$I_{TX,0dBm}$		-	25	-	mA	0dBm output power
$I_{RX,DCDC}$	Operating current in RX mode	-	12.5	-	mA	Max LNA gain in DCDC mode
$I_{RX,LDO}$		-	18	-	mA	Max LNA gain in LDO Mode
V_{OH}	Output high level voltage	VDD-0.3	-	VDD	V	-
V_{OL}	Output low level voltage	VSS	-	VSS+0.3	V	-
V_{IH}	Input high level voltage	0.8*VDD	-	-	V	-
V_{IL}	Input low level voltage	-	-	0.2*VDD	V	-
SPI_rate	SPI rate	-	-	10	Mbps	-

5.1.3 RF performance

Test Conditions:

- Supply voltage: 3.3V
- Temperature: 25℃
- Frequency: 490MHz
- Error Correction Code = 4/8
- Packet error rate ≤ 5%
- Payload length = 10Bytes

Table 5-3 RF parameters

Symbol	Description	Condition	Min	Typ	Max	Unit
General frequency						
F_{op}	Operating frequency	-	370	-	590	MHz
		-	740	-	1180	MHz
F_{xtal}	Crystal frequency	-	-	32	-	MHz
R_S	Crystal series resistance	-	-	30	50	Ω
C_{FOOT}	Crystal external capacitor	-	8	15	22	pF
C_{LOAD}	Crystal load capacitance	-	6	10	12	pF
F_{TOL}	Initial frequency tolerance	-	-	±10	-	ppm
BR	Bit rate		0.08	-	20.4	kbps
Transmitter						
P_{LPWAN}	Output Power	-	-7	-	22	dBm
Receiver						
RF_62.5	RF sensitivity, long range mode, highest LNA gain, 62.5 kHz bandwidth using separate RX/TX channels	SF = 7 SF = 10 SF = 12	- - -	-126 -135 -140	- - -	dBm
RF_125	RF sensitivity, long range mode, highest LNA gain, 125 kHz bandwidth using separate RX/TX channels	SF = 7 SF = 10 SF = 12	- - -	-124 -132 -137	- - -	dBm
RF_250	RF sensitivity, long range mode, highest LNA gain, 250 kHz bandwidth using separate RX/TX channels	SF = 7 SF = 10 SF = 12	- - -	-121 -129 -134	- - -	dBm
RF_500	RF sensitivity, long range mode, highest LNA gain, 500 kHz bandwidth using separate RX/TX channels	SF = 7 SF = 10 SF = 12	- - -	-119 -126 -132	- - -	dBm

Note:

- The above test data is based on the 490MHz frequency point. There are differences in other frequency band parameters.

5.2 2.4G

Note: The VDD and other parameters described in this section correspond to the power input pins such as "xxx_BLE" in the Pin Information.

5.2.1 Absolute maximum rating

Table 5-4 Absolute maximum rating

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VDD - VSS	Supply voltages	TA=25°C	-0.3	-	3.6	V
VIN	I/O pin voltage	TA=25°C	VSS-0.3	-	VDD + 0.3	V
PVDD	Extreme power consumption	VDD=3.3V, TA=25°C DCDC power supply	-	-	250	mW
T_{ST}	Storage temperature	-	-65	-	150	℃
T_A	Ambient temperature	-	-40	-	85	℃
T_J	Junction temperature	-		-	135	℃

5.2.2 General operating conditions

Table 5-5 General operating conditions

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VDD	Operating voltage	TA=25°C	1.8	-	3.6	V
VIPIO2	Operating voltage	TA=25°C	1.8	-	3.6	V

5.2.3 RF characteristics

Table 5-6 RF characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{OP}	Operating frequency		2400	-	2483	MHz
PLLres	PLL programming resolution		-	1	-	MHz
DR	Data rate		0.125	-	2	MHz
$\Delta f_{BLE,2M}$	Frequency deviation @ BLE 2Mbps		450	500	550	kHz
$\Delta f_{BLE,1M}$	Frequency deviation @ BLE 1Mbps		225	250	275	kHz
$\Delta f_{297,2M}$	Frequency deviation @ 297mode 2Mbps		450	500	550	kHz
$\Delta f_{297,1M}$	Frequency deviation @ 297mode 1Mbps		225	250	275	kHz
$\Delta f_{N,2M}$	Frequency deviation @ N-mode 2Mbps		-	320	-	kHz

$\Delta f_{N,1M}$	Frequency deviation @ N-mode 1Mbps		-	170	-	kHz
$\Delta f_{BLE,2M}$	Channel spacing @ BLE 2Mbps		-	2	-	MHz
$\Delta f_{BLE,1M}$	Channel spacing @ BLE 1Mbps		-	2	-	MHz
$\Delta f_{297,2M}$	Channel spacing @ 297mode 2Mbps		-	2	-	MHz
$\Delta f_{297,1M}$	Channel spacing @ 297mode 1Mbps		-	1	-	MHz
$\Delta f_{N,2M}$	Channel spacing @ N-mode 2Mbps		-	2	-	MHz
$\Delta f_{N,1M}$	Channel spacing @ N-mode 1Mbps		-	1	-	MHz

Table 5-7 TX characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
P_{RFTX}	Output power		-	-	7	dBm
P_{RFC}	RF power control range		-	40	-	dB
P_{RFCR}	RF power accuracy		-	-	±3	dB
$P_{RF1M,1}$	1st Adjacent Channel Transmit Power @1Mbps		-	-32	-	dB
$P_{RF1M,2}$	2nd Adjacent Channel Transmit Power @1Mbps		-	-49	-	dB
$P_{RF1M,\geqslant 3}$	3rd Adjacent Channel Transmit Power @1Mbps		-	-54	-	dB
$P_{RF2M,2}$	1st Adjacent Channel Transmit Power @2Mbps		-	-21.5	-	dB
$P_{RF2M,4}$	2nd Adjacent Channel Transmit Power @2Mbps		-	-48	-	dB
$P_{RF2M,\geqslant 6M}$	3rd Adjacent Channel Transmit Power @2Mbps		-	-53	-	dB
P_{BW1M}	20dB bandwidth @1Mbps		-	1.3	-	MHz
P_{BW2M}	20dB bandwidth @2Mbps		-	2.3	-	MHz
$P_{SP,1}$	Spurious @$\leqslant$1GHz		-	-	-63	dBm
$P_{SP,2}$	Spurious @$\geqslant$1GHz		-	-	-43	dBm

Table 5-8 RX characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$P_{RX,MIX}$	Receive maximum input power		-	0	-	dBm
$P_{SENS,BLE,1M}$	Sensitivity, 1Mbps BLE		-	-96	-	dBm
$P_{SENS,BLE,2M}$	Sensitivity, 2Mbps BLE		-	-93	-	dBm
$P_{SENS,BLE,125K}$	Sensitivity, 125Kbps BLE		-	-99	-	dBm
$P_{SENS,BLE,500K}$	Sensitivity, 500Kbps BLE		-	-99	-	dBm
$P_{SENS,297,1M}$	Sensitivity, 1Mbps 297mode		-	-95	-	dBm
$P_{SENS,297,2M}$	Sensitivity, 2Mbps 297mode		-	-92	-	dBm

$P_{SENS,N,1M}$	Sensitivity, 1Mbps N-mode		-	-95	-	dBm
$P_{SENS,N,2M}$	Sensitivity, 2Mbps N-mode		-	-92	-	dBm
$C/I_{CO,1M}$	Co-Channel interference@1Mbps		-	21	-	dB
$C/I_{1M,1M}$	Adjacent (1 MHz) interference@1Mbps		-	15	-	dB
$C/I_{2M,1M}$	Adjacent (2 MHz) interference @1Mbps		-	-17	-	dB
$C/I_{3M,1M}$	Adjacent (≥3 MHz) interference @1Mbps		-	-27	-	dB
$C/I_{Image,1M}$	Image frequency interference@1Mbps		-	-9	-	dB
$C/I_{Image±1M,1M}$	Adjacent (±1MHz) interference to in-band image frequency @1Mbps		-	-15	-	dB
$C/I_{≥6M,1M}$	Adjacent (≥6 MHz) interference @1Mbps		-	-27	-	dB
$C/I_{CO,2M}$	Co-Channel interference @2Mbps		-	21	-	dB
$C/I_{2M,2M}$	Adjacent (2 MHz) interference @2Mbps		-	15	-	dB
$C/I_{4M,2M}$	Adjacent (4 MHz) interference @2Mbps		-	-17	-	dB
$C/I_{6M,2M}$	Adjacent (≥6 MHz) interference @2Mbps		-	-27	-	dB
$C/I_{Image,2M}$	Image frequency interference @2Mbps		-	-9	-	dB
$C/I_{Image±2M,2M}$	Adjacent (±2 MHz) interference to in-band image frequency @2Mbps		-	-15	-	dB
$C/I_{≥12M,2M}$	Adjacent (≥12 MHz) interference @2Mbps		-	-27	-	dB
$C/I_{CO,125K}$	Co-Channel interference @125Kbps		-	12	-	dB
$C/I_{1M,1M125K}$	Adjacent (1 MHz) interference @125Kbps		-	6	-	dB
$C/I_{2M,1M125K}$	Adjacent (2 MHz) interference @125Kbps		-	-26	-	dB
$C/I_{≥3M,1M125K}$	Adjacent (≥3MHz) interference @125Kbps		-	-36	-	dB
$C/I_{Image,1M125K}$	Image frequency interference @125Kbps		-	-18	-	dB
$C/I_{Image±1M,125K}$	Adjacent (±1MHz) interference to in-band image frequency @125Kbps		-	-24	-	dB
$C/I_{CO,500K}$	Co-Channel interference @500Kbps		-	17	-	dB
$C/I_{1M,500K}$	Adjacent (1 MHz) interference @500Kbps		-	11	-	dB
$C/I_{2M,500K}$	Adjacent (2 MHz) interference @500Kbps		-	-21	-	dB
$C/I_{≥3M,500K}$	Adjacent (≥3MHz) interference @500Kbps		-	-31	-	dB
$C/I_{Image,500K}$	Image frequency interference @500Kbps		-	-13	-	dB
$C/I_{Image±1M,500K}$	Adjacent (±1MHz) interference to in-band image frequency @500Kbps		-	-19	-	dB
$P_{IMD,5TH,1M}$	IMD performance 5 MHz offset @1Mbps		-	-30	-	dBm
$P_{IMD,5TH,2M}$	IMD performance 10 MHz offset @2Mbps		-	-31	-	dBm

Table 5-9 RSSI characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$RSSI_{RFC}$	RSSI indication range		-90	-	-15	dBm
$RSSI_{Auu}$	RSSI accuracy		-	±2	-	dB
$RSSI_{Res}$	RSSI resolution		-	0.25	-	dB
$RSSI_{Per}$	RSSI Sample period		-	15	-	us

Table 5-10 RF Timing characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$T_{OSC,EN}$	Crystal oscillator settling time		-	230	-	us
$T_{TX,EN}$	Time between TXEN task and READY event after channel FREQUENCY configured		-	TBD	-	us
$T_{RX,EN}$	Time between the RXEN task and READY event after channel FREQUENCY configured in default mode		-	TBD	-	us
$T_{TX,DISABLE}$	Time between DISABLE task and DISABLED event when the radio was in TX		-	TBD	-	us
$T_{RX,DISABLE}$	Time between DISABLE task and DISABLED event when the radio was in RX		-	TBD	-	us
T_{RX-TX}	The time taken to switch from RX to TX or TX to RX		-	150	-	us

Table 5-11 RF power characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$I_{TX,P6dBm,DCDC}$	TX only run current 6dBm @ DC-DC		-	15.2	-	mA
$I_{TX,P4dBm,DCDC}$	TX only run current 4dBm @DC-DC		-	9.6	-	mA
$I_{TX,P0dBm,DCDC}$	TX only run current 0dBm @DC-DC		-	6.1	-	mA
$I_{TX,P-4dBm,DCDC}$	TX only run current -4dBm @DC-DC		-	4.6	-	mA
$I_{TX,P-8dBm,DCDC}$	TX only run current -8dBm @DC-DC		-	3.8	-	mA
$I_{TX,P-12dBm,DCDC}$	TX only run current -12dBm @DC-DC		-	3.3	-	mA
$I_{TX,P-16dBm,DCDC}$	TX only run current -16dBm @DC-DC		-	3	-	mA
$I_{TX,P-20dBm,DCDC}$	TX only run current -20dBm @DC-DC		-	2.8	-	mA
$I_{TX,P-40dBm,DCDC}$	TX only run current -40dBm @DC-DC		-	2.2	-	mA
$I_{TX,P6dBm,LDO}$	TX only run current 6dBm @LDO		-	29.2	-	mA
$I_{TX,P4dBm,LDO}$	TX only run current 4dBm @LDO		-	16.6	-	mA
$I_{TX,P0dBm,LDO}$	TX only run current 0dBm @LDO		-	10.6	-	mA

$I_{TX,P-4dBm,LDO}$	TX only run current -4dBm @LDO		-	7.6	-	mA
$I_{TX,P-8dBm,LDO}$	TX only run current -8dBm @LDO		-	6.4	-	mA
$I_{TX,P-12dBm,LDO}$	TX only run current -12dBm @LDO		-	5.6	-	mA
$I_{TX,P-16dBm,LDO}$	TX only run current -16dBm @LDO		-	5.1	-	mA
$I_{TX,P-20dBm,LDO}$	TX only run current -20dBm @LDO		-	4.8	-	mA
$I_{TX,P-40dBm,LDO}$	TX only run current -40dBm @LDO		-	3.7	-	mA
$I_{RX,1M,DCDC}$	RX 1Mbps current @DC-DC		-	5.6	-	mA
$I_{RX,2M,DCDC}$	RX 2Mbps current @DC-DC		-	5.9	-	mA
$I_{RX,1M,LDO}$	RX 1Mbps current @LDO		-	9.6	-	mA
$I_{RX,2M,LDO}$	RX 2Mbps current @LDO		-	10.5	-	mA

Test conditions and methods.
1.Transceiver power consumption tested in 1M mode using BLE ADV broadcast mode
2.2M mode is used is the power consumption when BLE connection
3.The power consumption tested is the RF peak power
4.The test method uses the total power consumption minus the power consumption of the MCU when the RF is not operating to calculate the final power consumption
5.The sample software tested is based on peripheral_hr

5.2.4 GPIO characteristics

Table 5-12 GPIO characteristics (single IO)

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{IH}	Input high voltage	TA=25°C	0.48*VDD	-	VDD	V
V_{IL}	Input low voltage	TA=25°C	VSS	-	VSS+0.24*VDD	V
V_{HYS}	Input hysteresis voltage, $V_{hys}=V_{IH}-V_{IL}$	TA=25°C	-	-	0.24*VDD	V
C_{Iana}	Analog input capacitors	Load capacitance =20pF, TA=25°C	-	300	-	fF
I_{Lkg}	Leakage current, open-drain mode or input mode	VDD ≤ VIN ≤ 3.6V	-	-	2.5	uA
R_{PU}	Pull-up resistor	Vin =Vss, Vdd =3.3V	48	50	52	kΩ
R_{PD}	Pull-down resistor	Vin =Vss, Vdd =3.3V	98	100	102	kΩ
V_I	Input voltage	TA=25°C	VSS	-	VDD	V
$V_{I,P40-P44}$	Input voltage	TA=25°C	VSS	-	VIPIO2	V
V_O	Output voltage	TA=25°C	VSS	-	VDD	V
$V_{O,P40-P44}$	Output voltage	TA=25°C	VSS	-	VIPIO2	V
I_{OH}	Source current （Push-pull output）	Vin =Vdd-0.5V	4.2	8	8.5	mA
	Source current		9	10	11	mA

	（Quasi-bidirectional, high）					
I_{Sink}	Sink current（Push-pull output）	Vin =Vss+0.5V，TA=25°C	12	16	25	mA
f_{Port_CLK}	IO output frequency	Load capacitance =20pF	-	-	64	MHz

Table 5-13 Combined test

Description	Conditions	Status	Remark
IO default state after power on	VDD=3.3V ,TA=25°C	P46, P47 pull-up input state, other GPIOs are high resistance state	
IO status in deepsleep mode	VDD=3.3V ,TA=25°C	Under M0 except P56, P46, P47 (available), the rest are high resistance state, IO can be held	
IO status at reset	VDD=3.3V ,TA=25°C	P46, P47 pull-up input state, other GPIOs are high resistance state	

Table 5-14 nRESET Input Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{ILR}	Negative threshold voltage, nRESET	VDD=1.8V-3.3V ,TA=25°C	-	-	0.22*VDD	V
V_{IHR}	Positive threshold voltage, nRESET	VDD=1.8V-3.3V ,TA=25°C	0.48*VDD	-	-	V
V_{hys_rst}	Schmitt Trigger Voltage Hysteresis	VDD=1.8V-3.3V ,TA=25°C	-	-	0.26*VDD	V
R_{RST}	nRESET pin internal pull-up resistor	VDD=3.3V ,TA=25°C	4.6	4.8	5	kΩ
$t_{FR,\ 0.3pF}$	nRESET pin input filter pulse time	VDD=3.3V ,TA=25°C	-	20	-	ns

5.2.5 Reset characteristics

Table 5-15 Reset characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{BOD}	Brown-out detection voltage threshold	BODSEL<2:0> = 000(rising edge)，dVDD/dt≤3V/s	-	2.19	-	V
		BODSEL<2:0> = 000(falling edge)，dVDD/dt≤3V/s	-	2.08	-	
		BODSEL<2:0> = 001(rising edge)，dVDD/dt≤3V/s	-	2.4	-	
		BODSEL<2:0> = 001(falling edge)，dVDD/dt≤3V/s	-	2.29	-	
		BODSEL<2:0> = 010(rising edge)，dVDD/dt≤3V/s	-	2.65	-	
		BODSEL<2:0> = 010(falling edge)，	-	2.53	-	

		dVDD/dt≤3V/s				
		BODSEL<2:0> = 011(rising edge)，dVDD/dt≤3V/s	-	2.85	-	
		BODSEL<2:0> = 011(falling edge)，dVDD/dt≤3V/s	-	2.72	-	
		BODSEL<2:0> =100(rising edge)，dVDD/dt≤3V/s	-	3.09	-	
		BODSEL<2:0> = 100(falling edge)，dVDD/dt≤3V/s	-	2.95	-	
		BODSEL<2:0> = 101(rising edge)，dVDD/dt≤3V/s	-	3.33	-	
		BODSEL<2:0> = 101(falling edge)，dVDD/dt≤3V/s	-	3.17	-	
V_{BODhys}	BOD hysteresis voltage	dVDD/dt≤3V/s	100	-	160	mV
T_{BOD_RE1}	BOD response Time, Normal mode	dVDD/dt≤3V/s	2^4	2^4	2^15	1/SYS_CLK
I_{BOD}	BOD operating current	dVDD/dt≤3V/s	-	5	-	uA
V_{POR}	Power on reset voltage threshold	Rising edge, dvdd/dt≤3V/s	-	1.7	-	V
		Falling edge, dvdd/dt≤3V/s	-	1.7	-	V
T_{POR}	POR settling time	Vbat =3.3v	-	1.5	6.4	ms
V_{LVR}	LVR detection voltage threshold	Falling edge, dvdd/dt≤3V/s	-	1.93	-	V
T_{LVR_RE}	LVR response time	TA=25°C, dVDD/dt≤3V/s	2^4	2^4	2^15	1/SYS_CLK
I_{LVR}	LVR operating current	TA=25°C, dVDD/dt≤3V/s	12.2	-	18.5	uA

5.2.6 Clock characteristics

Table 5-16 HXTAL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{HXTL}	High speed crystal oscillator (HXTAL) frequency	VDD=3.3V ,TA=25°C	-	32	-	MHz
$C_{LoadHXTL}$	Crystal load capacitance	VDD=3.3V ,TA=25°C	-	12	-	pF
I_{DDHXTL}	HXTAL oscillator operating current	VDD=3.3V ,TA=25°C	-	-	250	μA
t_{SUHXTL}	HXTAL oscillator startup time	VDD=3.3V ,TA=25°C, ESR=70Ω, C_{HXTL}= 13pF	-	200	-	μs
$t_{SUHXTL\ Quick}$	HXTAL oscillator Quick startup time	VDD=3.3V ,TA=25°C, ESR=70Ω, C_{HXTL}= 13pF	-	150	-	μs
ESR			-	50	80	Ω
OA_{HXTL}	Oscillation margin of HF crystals	VDD=3.3V ,TA=25°C	-	250	-	Ω

Table 5-17 LXTAL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{LXTL}	Low speed crystal oscillator (LXTAL) frequency	VDD=3.3V ,TA=25°C	-	32.768	-	kHz
I_{DDLXTL}	LXTAL oscillator operating current	VDD=3.3V ,TA=25°C	-	0.76	-	μA
t_{SULXTL}	LXTAL oscillator Normal startup time	VDD=3.3V ,TA=25°C	-	200	-	ms
$t_{SULXTL\ Quick}$	LXTAL oscillator Quick startup time	VDD=3.3V ,TA=25°C	-	2	-	ms
ESR_{LXTL}	Equivalent series resistance 6 pF < CL ≤ 9 pF	VDD=3.3V ,TA=25°C	-	100	-	kΩ
OA_{LXTL}	Oscillation margin of LF crystals	VDD=3.3V ,TA=25°C	-	440	-	kΩ
$C_{LoadXTL}$	Crystal load capacitance	VDD=3.3V ,TA=25°C	-	12	-	pF

Table 5-18 32MHz RCH characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{IRC32M}	Crystal frequency	VDD=3.3V ,TA=25°C	-	32	-	MHz
ACC_{IRC32M}	Frequency accuracy	VDD=3.3V, TA=-40°C ~+105°C	-	-	-	%
		VDD=3.3V, TA=-20°C ~ +85°C	-	-	-	%
		VDD=3.3V, TA=25°C	-2	1	2	%
D_{IRC32M}	IRC32M oscillator duty cycle	VDD=3.3V, f_{IRC32M}=32MHz, TA=25°C	48	50	52	%
$I_{DDIRC32M}$	Operating current	VDD=3.3V, f_{IRC8M}=32MHz, TA=25°C	200	390	480	μA
$t_{SUIRC32M}$	Startup time	VDD=3.3V, f_{IRC32M}=32MHz, TA=25°C	-	5	-	μs
$d_{fIRC32M}$	25°C, The frequency drifts with the supply voltage	VDD=1.8V~3.6V, TA=25°C	-	0.5	-	%/V

Table 5-19 32kHz RCL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{IRC32k}	Crystal frequency	VDD=3.3V ,TA=25°C	-	32	-	kHz
ACC_{IRC32K}	Frequency accuracy	VDD=3.3V, TA=-40°C ~ +105°C (After calibration）	-	2000	-	ppm
D_{IRC32K}	IRC32K oscillator duty cycle	VDD=3.3V, f_{IRC32K}=32kHz, TA=25°C	7	-	16	%
$I_{DDIRC32K}$	Operating current	VDD=3.3V, f_{IRC8K}=32kHz, TA=25°C	-	700	-	nA
$t_{SUIRC32K}$	Startup time	VDD=3.3V, f_{IRC32K}=32kHz, TA=25°C	-	-	200	μs

df_{IRC32K}	25°C, The frequency drifts with the supply voltage	VDD=1.8V~3.6V, TA=25°C	-	5.5	-	%/V

Table 5-20 DPLL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{PLLIN}	PLL input clock frequency	VDD=3.3V, TA=25°C	-	32	-	MHz
f_{PLL}	PLL output clock frequency	VDD=3.3V, TA=25°C	48	48	64*	MHz
I_{PLL}	Operating current	VDD=3.3V, TA=25°C	-	330	-	μA

Note: VDD needs to be above 2V.

5.2.7 ADC characteristics

Table 5-21 Power supply and input range conditions

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$V_{Ax(VBG\ adc)}$	Analog input voltage range, VBG（1.2V）	VDD=3.3V, TA=25°C	0	-	VBG_{ADC}	V
$V_{Ax(VDD)}$	Analog input voltage range, VDD	VDD=3.3V, TA=25°C	0	-	VDD	V
I_{ADC}	ADC supply current	VDD=3.3V, TA=25°C Fadc=16MHz	-	0.5	-	mA
C_{sample}	Internal sample and hold capacitors (PAD and PCB capacitors not included)		-	12	-	pF
R_{ADC}	Sampling switch resistance	0V ≤ VAx ≤ VDD	-	300	-	Ω
R_{In}	External input impedance, continuous sampling	0V ≤ VAx ≤ VDD	0.86	-	4734.70	kΩ

Table 5-22 ADC built-in voltage reference

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VBG_{ADC}	Internal 1.2V Reference Voltage	VDD=3.3V, TA=25°C	1.1	1.2	1.3	V
T_{Coef}	Temperature factor	TA=-40°C~105°C; VDD=1.8V~3.6V	-	-1	-	mV/°C

Table 5-23 Time parameters

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
F_{ADC}	ADC clock frequency	VDD=3.3V, TA=25°C	4	16	32	MHz

T_S	Sample time	VDD=3.3V, TA=25°C	4	1539	8192	$1/F_{adc}$
T_{CONV}	Conversion time	VDD=3.3V, TA=25°C	32	1580	8298	$1/F_{adc}$

Table 5-24 Linearity parameter

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
INL	Integral linearity error	VDD=3.3V, TA=25°C	-	-	±3	LSB
DNL	Differential linearity error	VDD=3.3V, TA=25°C	-	-	±3	LSB
SNR	Signal to Noise Ratio	Fadc = 16MHz Input Clock 250kHz VDD=3.3V, TA=25°C	-	64.3	-	dB
THD	Total harmonic distortion		-	75	-	dB
SFDR	Spurious-free signal dynamic range		-	77.29	-	dB
ENOB	Effective number of bits		-	10.33	-	Bit

Table 5-25 Temperature Sensor

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
T_{range}	Range	VDD=3.3V	-40	25	125	℃
Avg_{Slope}	Average slope	VDD=3.3V	-1.46	-2	-2.55	CODE/℃

Table 5-26 RIN

ADC significant bit	F_{ADC}(MHz)	Ts(cycles)	Ts(us)	Rinmax(kΩ)
12	32	4	0.125	0.86
12	32	8	0.25	2.01
12	32	32	1	8.95
12	32	64	2	18.20
12	32	128	4	36.69
12	32	8192	256	2367.20
12	16	4	0.25	2.01
12	16	8	0.5	4.32
12	16	32	2	18.20
12	16	64	4	36.69
12	16	128	8	73.68
12	16	8192	512	4734.70

Note: The sampling condition is continuous sampling.

5.2.8 PMU characteristics

Table 5-27 PMU characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{HLDO}	HLDO output voltage range, external capacitor	VDD=3.3V, TA=25°C	1.1	1.2	1.3	V
VDD_{PSRR}	Power supply rejection ratio of VDD	VDD=3.3V, TA=25°C	-15	-	-	dB

Note: DCDC-OFF

5.2.9 DCDC characteristics

Table 5-28 DCDC characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{IN_DCDC}	Input voltage range	VDD=3.3V, TA=25°C	2	-	3.6	V
V_{OUT_DCDC}	Output voltage range	VDD=3.3V, TA=25°C	-	1.5	1.8	V
T_{EN_DCDC}	Standup time	VDD=3.3V ,I_{LOAD}=10mA, TA=25°C	-	200	-	us
η	Efficiency	VDD=3.3V ,I_{LOAD}=10mA, TA=25°C， L_{DCR}=80mΩ	-	83	-	%
$VRPL_{DCDC}$	Ripple	VDD=3.3V, TA=25°C	-	50	-	mv
I_{OUT}	Drive peak current	VDD=3.3V, TA=25°C	-	-	150	mA
I_{AVG}	Drive average current	VDD=3.3V, TA=25°C	-	-	30	mA
L_{DCDC}	Effective inductance	VDD=3.3V, TA=25°C	-	2.2	-	μH
C_{OUT_DCDC}	Effective load capacitance	VDD=3.3V, TA=25°C	-	4.7	-	μF
F_{osc_DCDC}	Oscillation frequency	VDD=3.3V, TA=25°C	100	-	1000	kHz

5.2.10 MCU current characteristics

Symbol	Parameter	Conditions		DCDC ON	DCDC OFF
				Typ(mA)	Typ(mA)
Run mode	All peripherals clockon, run while(1) in flash	System clock source: RCH	4M	0.786	1.1
			8M	1.35	1.93
			16M	2.1	3.05
			32M	3.61	5.43
		System clock source: XTH	4M	1.36	1.97
			8M	1.93	2.8
			16M	2.68	3.93
			32M	4.19	6.18
		System clock source: DPLL	16M	3.18	4.67
			24M	3.93	5.78
			32M	4.7	6.95

			48M	6.21	9.18
			64M	7.7	11.44
	All peripherals clockoff, run while(1) in flash	System clock source：RCH	4M	0.75	1.05
			8M	0.92	1.31
			16M	1.24	1.79
			32M	1.86	2.69
		System clock source：XTH	4M	1.05	1.5
			8M	1.22	1.75
			16M	1.57	2.26
			32M	2.23	3.25
		System clock source：DPLL	16M	1.86	2.7
			24M	2.2	3.21
			32M	2.57	3.76
			48M	3.25	4.77
			64M	3.97	5.84

Notes: Test conditions - DVDD=1.2V, VDD=3.3V, VBG=1.2V, TA=25°C

Symbol	Parameter	Conditions		Typ(μA)
standby m0	all sram lost	wake by 32k timer	RCL	1.14
			XTL	1.14
		wake by gpio p56		0.34
standby m1	all sram lost	wake by 32k timer	RCL	1.39
			XTL	1.39
		wake by gpio p56		0.59
	all sram retention	wake by 32k timer	RCL	4.62
			XTL	4.62
		wake by gpio p56		3.99
	sram0 32k on	wake by 32k timer	RCL	2.41
			XTL	2.41
		wake by gpio p56		1.7
	sram1 16k on	wake by 32k timer	RCL	1.98
			XTL	1.98
		wake by gpio p56		1.26
	sram2 8k on	wake by 32k timer	RCL	1.76
			XTL	1.76
		wake by gpio p56		1
	sram3 8k on	wake by 32k timer	RCL	1.76
			XTL	1.76
		wake by gpio p56		1
	LL sram retention	wake by 32k timer	RCL	2.2
			XTL	2.2
		wake by gpio p56		1.46
	Decrypt sram retention	wake by 32k timer	RCL	1.47
			XTL	1.47

		wake by gpio p56		0.73
Deepsleep	all sram lost	wake by 32k timer	RCL	1.36
		wake by external P56		0.59
	all sram retention	wake by 32k timer	RCL	8.19
		wake by external P56		7.62
		wake by gpio all		7.57
		wake by peripheral timer	RCL+TIMER	8.41
		wake by peripheral wdt	RCL+WDT	8.43
		wake by peripheral kscan	RCL+KSCAN	8.59
		wake by peripheral qdec	RCL+QDEC	8.45
	sram0 32k on	wake by 32k timer	RCL	9.18
		wake by external P56		8.83
	sram1 16k on	wake by 32k timer	RCL	8.78
		wake by external P56		8.34
	sram2/sram3 8k on	wake by 32k timer	RCL	8.53
		wake by external P56		8.07
	LL sram retention	wake by 32k timer	RCL	8.98
		wake by external P56		8.57
	Decrypt sram retention	wake by 32k timer	RCL	8.25
		wake by external P56		7.81

Notes: Test conditions - DVDD=1.2V, VDD=3.3V, VBG=1.2V, TA=25°C

6 Application Reference Diagram

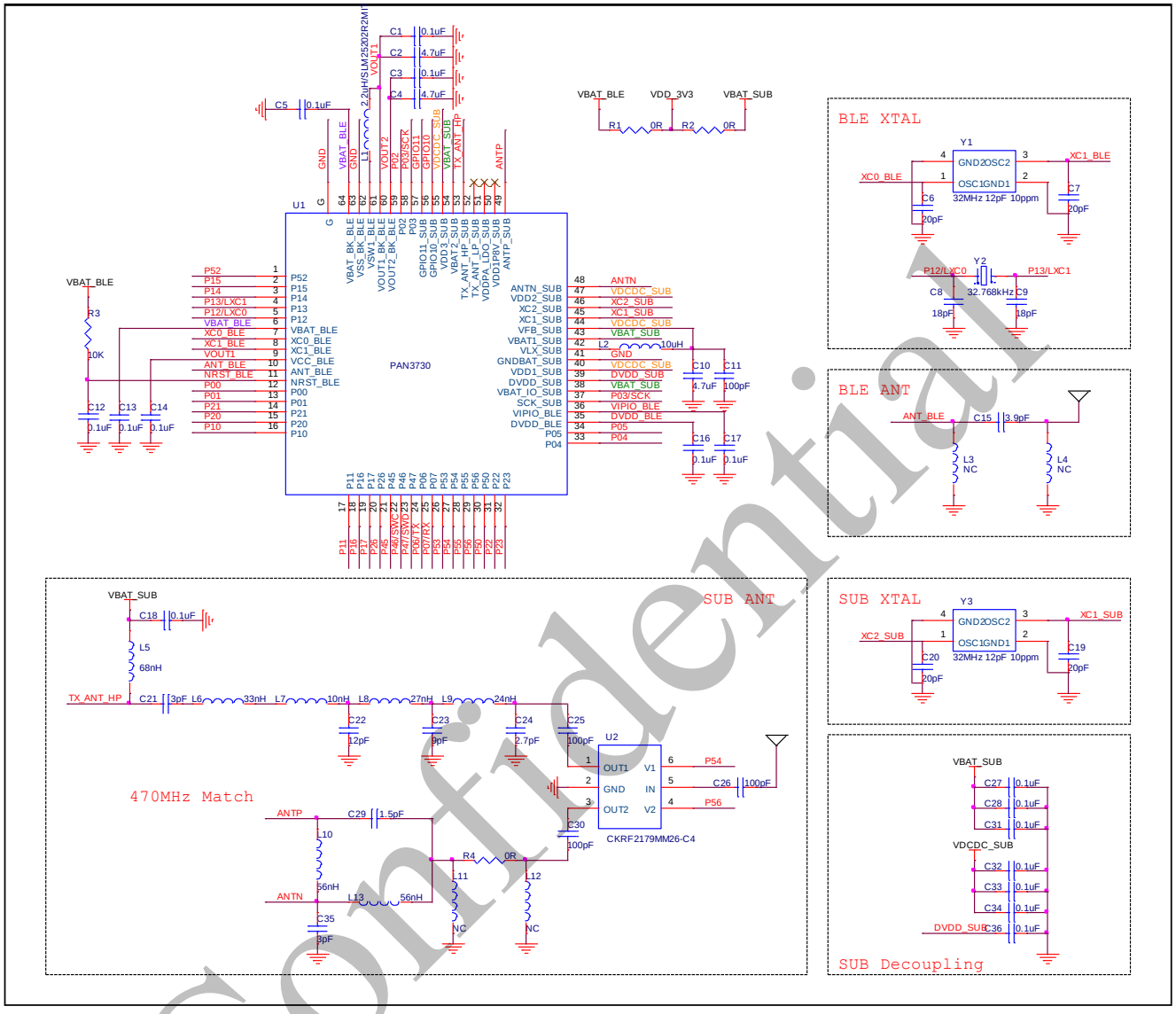


Figure 6-1 Application Schematic

7 Package Dimensions

7.1 QFN64 package

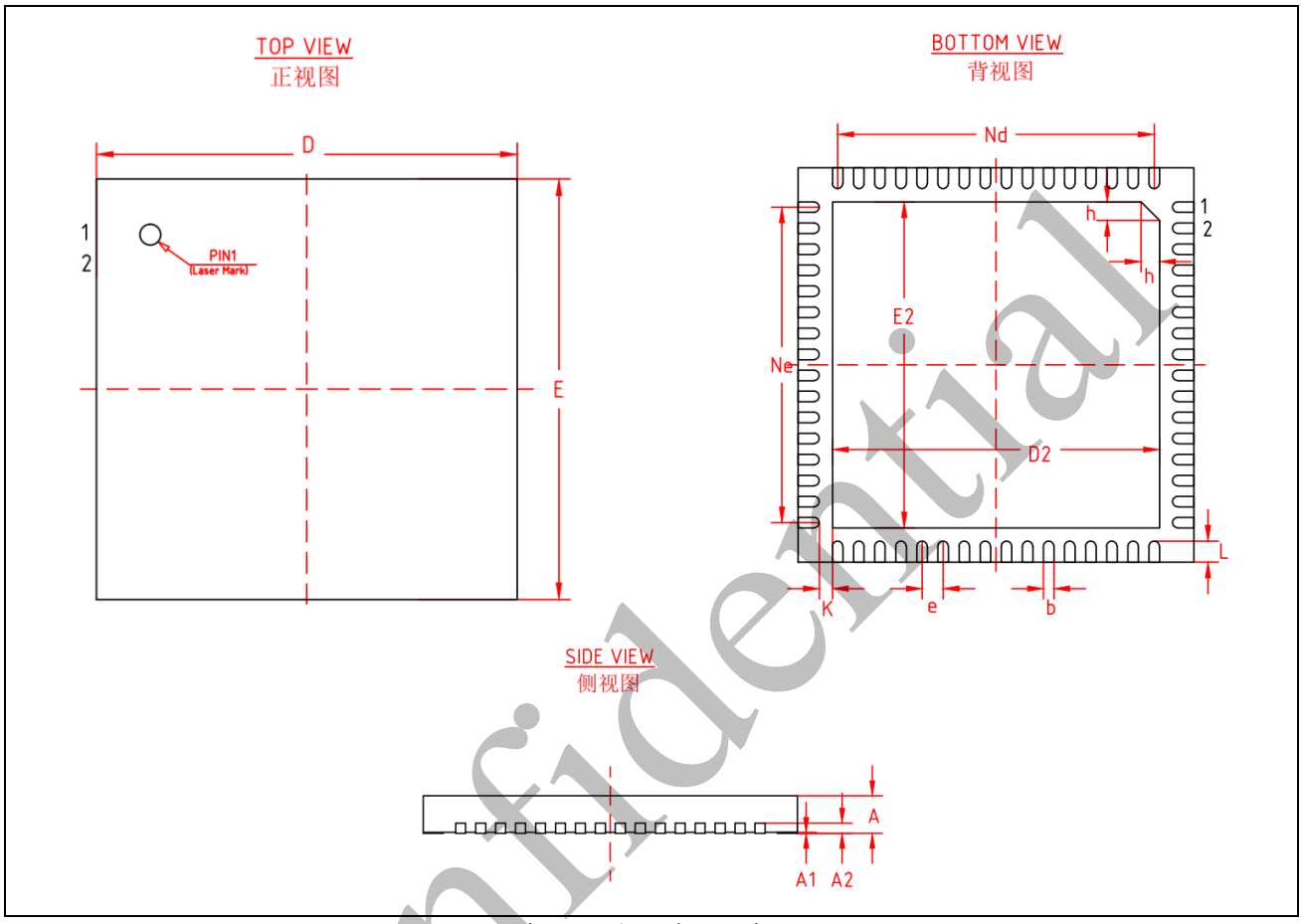


Figure 7-1 Package View

Table 7-1 Package Dimension

SYMBOL	MIN（mm）	NOM（mm）	MAX（mm）
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2	0.203 REF		
b	0.15	0.20	0.25
D	7.40	7.50	7.60
D2	6.15	6.20	6.25
E	6.90	7.50	7.60
E2	6.15	6.20	6.25
e	0.40 BSC		
K	0.20	0.25	0.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
Ne	6.00 BSC		
Nd	6.00 BSC		

8 Precautions

1. This product is a CMOS device and should be protected against static electricity during storage, transportation and use.
2. Grounding when device is in use.
3. Reflow temperature can not exceed 260℃.

   The lead-free reflow soldering process is shown in the figure below:

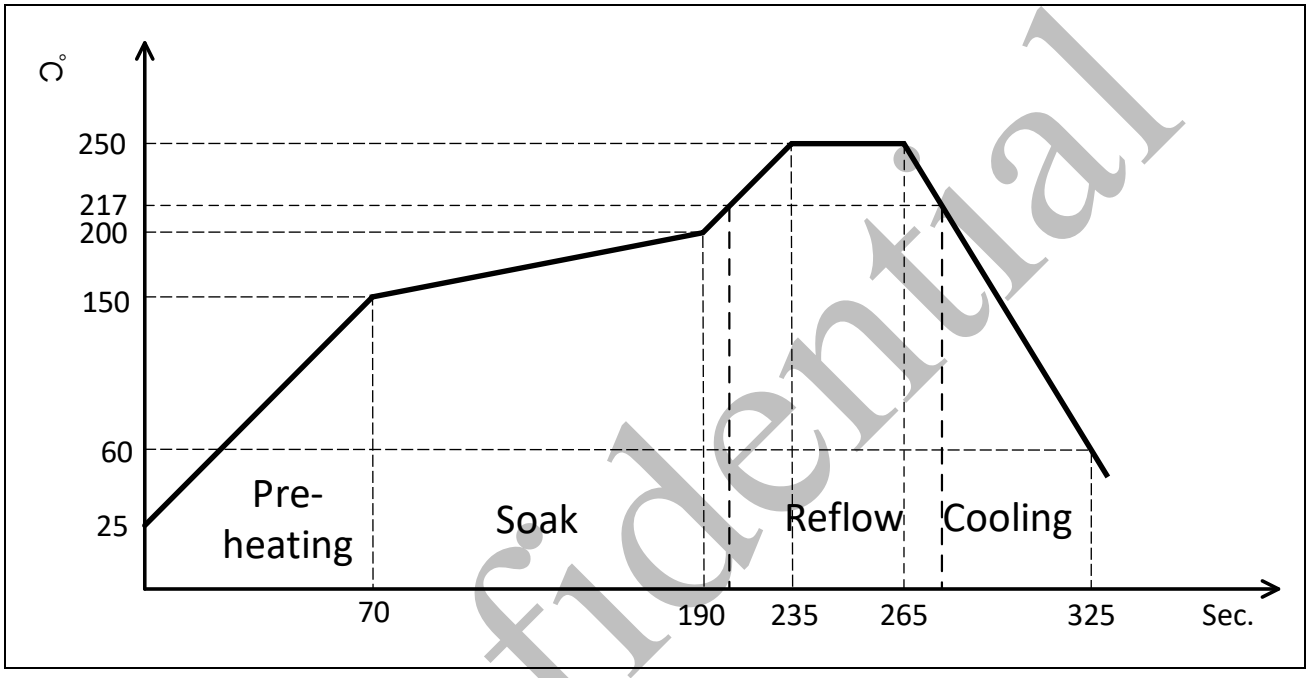


Figure 8-1 Reflow Profile

9 Storage Conditions

1. Products should be stored in sealed packages: when the temperature is less than 30 degrees and the humidity is less than 90%, it can last for 12 months.
2. After the package is opened, the components will be used in the reflow process or other high-temperature processes. The following conditions must be met:
   a. Completed within 72 hours and the factory environment is less than 30℃≤ 60% RH.
   b. Stored in 10% RH environment.
   c. Exhaust at 125℃ for 24 hours to remove internal water vapor before used.
3. MSL (Moisture Sensitivity Level): Level-3 (based on IPC/JEDEC J-STD-020)

Abbreviation

ACK	Acknowledge Signal
ADC	Analog-to-Digital Converter
BLE	Bluetooth Low Energy
BOD	Brown-out Detector
BQB	Bluetooth Qualification Body
CAD	Channel Activity Detection
CDM	Charged Device Model
CS	Chip Select
CTS	Clear to Send
DAC	Digital to Analog Converter
DCDC	DC-to-DC converter
DMA	Direct Memory Access
DPLL	Digital Phase Locked Loop
ECC	Elliptic Curve Cryptography
ESD	Electro-Static discharge
ext	External IO Port
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FMC	Flash Controller
FIFO	First Input First Output
GPIO	General-purpose I/O
HBM	Human-Body Model
HLDO	High Voltage Low-dropout regulator
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IAP	In-Application-Programming
IRQ	Interrupt ReQuest
LDO	Low Dropout Regulator
LED	Light-Emitting Diode
LVR	Low Voltage Reset
MAC	Media Access Control Layer
MCU	Microcontroller Unit
MISO	Master Input Slave Output
MM	Machine Model
MOSI	Master Output Slave Input
PLL	Phase Locked Loop
POR	Power-on Reset
PWM	Power-on Reset
QDEC	QuadDec
RAM	Random Access Memory
trg	Trigger
OSC	Oscillator
PA	Power Amplifier
RC	Resistor-Capacitor Oscillator
RF	Radio Frequency
PLL	Phase Locked Loop
RSSI	Received Signal Strength Indication
RX	Receiver
SDA	Serial Data
SF	Spreading Factor
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
STB	Standby mode
TEMP	Temperature Sensor
TX	Transmitter
RTS	Request To Send
UART	Universal Asynchronous Receiver/Transmitters
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer
XTAL	External Crystal
VCO	Voltage Controlled Oscillator

Revision History

Version	Date	Content
1.0	Feb.2023	Initial

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