PANCHIP

PAN107x series

Datasheet

V1.6 May. 2024

Panchip Microelectronics Co., Ltd.

BLE SoC Transceiver

General Description

PAN107x series integrates BLE5.3 and 2.4GHz dual-mode wireless SoC transceiver. The transceiver works in the 2.400-2.483GHz universal ISM frequency band. There is a 512KB Flash program memory and a 48KB SRAM memory. In addition, PAN107x series is equipped with a wealth of peripherals, including up to 21 GPIOs, 8-channel PWM, one 32-bit timer, two 24-bit timers, one I2C, two UARTs, two SPIs, seven external channels ADC, WDT, WWDT, USB2.0(Full Speed), 32K RC etc. PAN107x series is suitable for application of wireless mouse, smart home and electronic shelf label, BLE-AOA indoor locating.

Key Features

- **MCU**
  - 32-bit MCU core running up to 48MHz
- **Memory**
  - 512KB flash supporting deep power-down mode
  - 48KB SRAM
  - 128B eFuse
  - 4KB I-cache
- **Low Power**
  - Active mode RX: 2.5mA@1Mbps DCDC
  - Active mode TX at 0dBm: 5.06mA(DCDC)
  - Standby mode : 0.28uA
  - Standby mode(32K SRAM retention): 1.78uA(GPIO, XTL, RCL can wake up)
  - Deep sleep mode: 3.37uA(All Logic Retention, GPIO, XTL, RCL can wake up)
- **Clock**
  - 32MHz RC
  - 32MHz XTAL
  - 32kHz RC
  - 32.768kHz XTAL
  - DPLL(48MHz)
- **RF**
  - Mode
    - BLE5.3 modes: 1Mbps, 2Mbps, 500kbps, 125kbps
    - 2.4G private protocol: 1Mbps, 2Mbps, 500kbps, 250kbps, 125kbps, supporting hardware ACK
  - Output power: up to 9dBm
  - Receiver
    - -99dBm@125kbps
    - -99dBm@500kbps
    - -96dBm@1Mbps
    - -93dBm@2Mbps
  - RSSI
    - Resolution: 0.25dB
    - Accuracy: ±2dB
    - Range: -90dbm ~ -15dBm
  - Single antenna supported
  - Safety regulations: BQB / ETSI / FCC
  - Broadcast and Scan each 37 38 39 Channel per time in one second. The average power is about 13 uA.
- **Peripheral**
  - Up to 21 GPIOs
  - 8-channel PWM
    one 32-bit timer, two 24-bit timers
  - One I2C
  - Two UARTs
  - Two SPIs
  - 2-channel DMA
  - 12-channel ADC (7 ext, VBG_1P2, VBG_VT, 1/4VDD, VBG_0P6, Temp2)
  - WDT / WWDT
  - IO / BOD / POR / LVR / System reset
  - FMC(Support IAP, support the boot loader with address 0x0)
  - Clock measurement and clock calibration
  - USB2.0(Full_speed)
  - Flash data encryption
- **Temperature sensor**
  - Support temperature sensor
  - Test range: -40℃ ~ 85℃
- **Power Management**
  - Integrated voltage regulator
  - Operating voltage: 1.8V to 3.6V (Support DCDC)
- **Package**
  - QFN32 / QFN20
- **Operating Condition**
  - Operating temperature: -40℃ ~ 85℃ / -40℃ ~ 105℃
  - Storage temperature: -60℃~150℃

Typical Applications

- Electronic Shelf Label
- Wireless mouse
- LED light control

Bluetooth Features

Bluetooth Low Energy Controller

The PAN107x series Bluetooth Low Energy Controller supports all low-energy features required by Bluetooth specification version 5.3. The controller supports the following:

- **Support 1M PHY, 2M PHY and Coded PHY (s2 and s8)**
- **Support Advertising, Scanning, Initiating and Connection (both of Central and Periph-eral) role**
- **Up to 6 Link Layer state machines concurrently:**
  - 1 * Passive Scanning
  - 1 * Non-connectable advertising
  - 4 * Any other combinations (Legacy/Extended/Periodic Adverstising, Scanning and Connection)
- **Support LE Features:**
  - LL Encryption
  - LE Data Packet Length Extension
  - LL Privacy
  - Extended Scanner Filter Policies
  - LE Extended and Periodic Adverstising
  - Channel Selection Algorithm #2
  - Constant Tone Extension
- **Support Update Channel Statistics**

Bluetooth Host

- **Generic Access Profile (GAP) with all possible LE roles**
  - Peripheral & Central
  - Observer & Broadcaster
- **GATT (Generic Attribute Profile)**
  - Server (to be a sensor)
  - Client (to connect to sensors)
- **Pairing support, including the Secure Connections feature from Bluetooth 4.2**
- **Non-volatile storage support for permanent storage of Bluetooth-specific settings and data**
- **Clean HCI driver abstraction**
  - 3-Wire (H5) & 5-Wire (H4) UART
  - SPI
  - Local controller support as a virtual HCI driver

Bluetooth Mesh

- **Compatible with Bluetooth SIG Mesh Profile 1.0.1**
- **Support Mesh Provisioning**
- **Provisioner: PB-ADV**
- **Provisionee: PB-ADV, PB-GATT and PB-Remote**
- **Support Mesh Node Feature: Relay, Proxy, Friend, LPN**
- **Support Mesh Models**
  - SIG Models: Config Model, Health Model and Generic Models (Onoff and Light Con-trol Models)
  - SIG Developing Models: PB-Remote Model and SIG OTA Model
- **Support multiple smart speakers control concurrently for BaiDu Xiaodu, Alibaba Ali-genie and Amazon Echo**
- **Support network control: HeartBeat, Subnet, Secure Beacon and Group Control**
- **Support switch control for over 256 nodes without delay**
- **Mesh Security**
  - Provisioning: FIPS P-256 Elliptic Curve
  - Message: AES-CCM Encryption
  - Network: SEQ Control, IV Index and Key Fresh

Proprietary Radio 2.4G Features

- Support 250K, 1M and 2M PHY
- XN297L, PAN1026 protocol compliant
- Support No Acknowledge, Acknowledge and Acknowledge with payload
- Support CRC8, CRC16 and CRC24
- Support whitening
- Compatible with Bluetooth frame structure, can simulate Bluetooth broadcast and scanning
- Compatible with Bluetooth CODED PHY S2/S8
- Supports 2-byte address
- Support the same spread spectrum function as the BLE protocol

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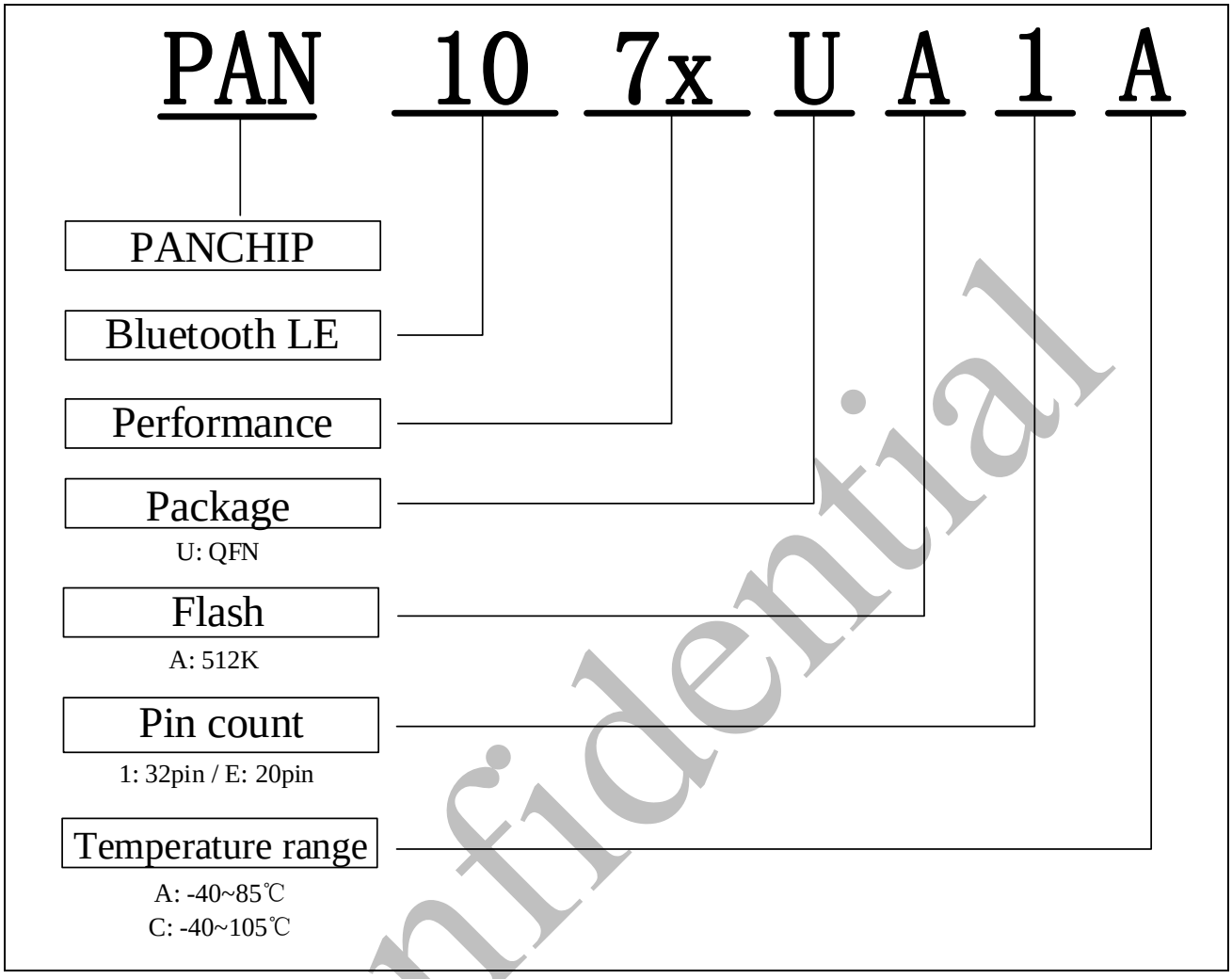
1 Naming rule



2 Ordering information

Partnumber	Type	Pack-age	Pin Count	IO	FLASH	RAM	Temperature range	Packing
PAN1070UA1A	BLE5.3	QFN	32	21	512K	48K	-40~85℃	Tape & Reel
PAN1070UA1C	BLE5.3	QFN	32	21	512K	48K	-40~105℃	Tape & Reel
PAN1070UAEC	BLE5.3	QFN	20	8	512K	48K	-40~105℃	Tape & Reel

Before ordering, please contact the sales window for the latest mass production information.

3 Block Diagram

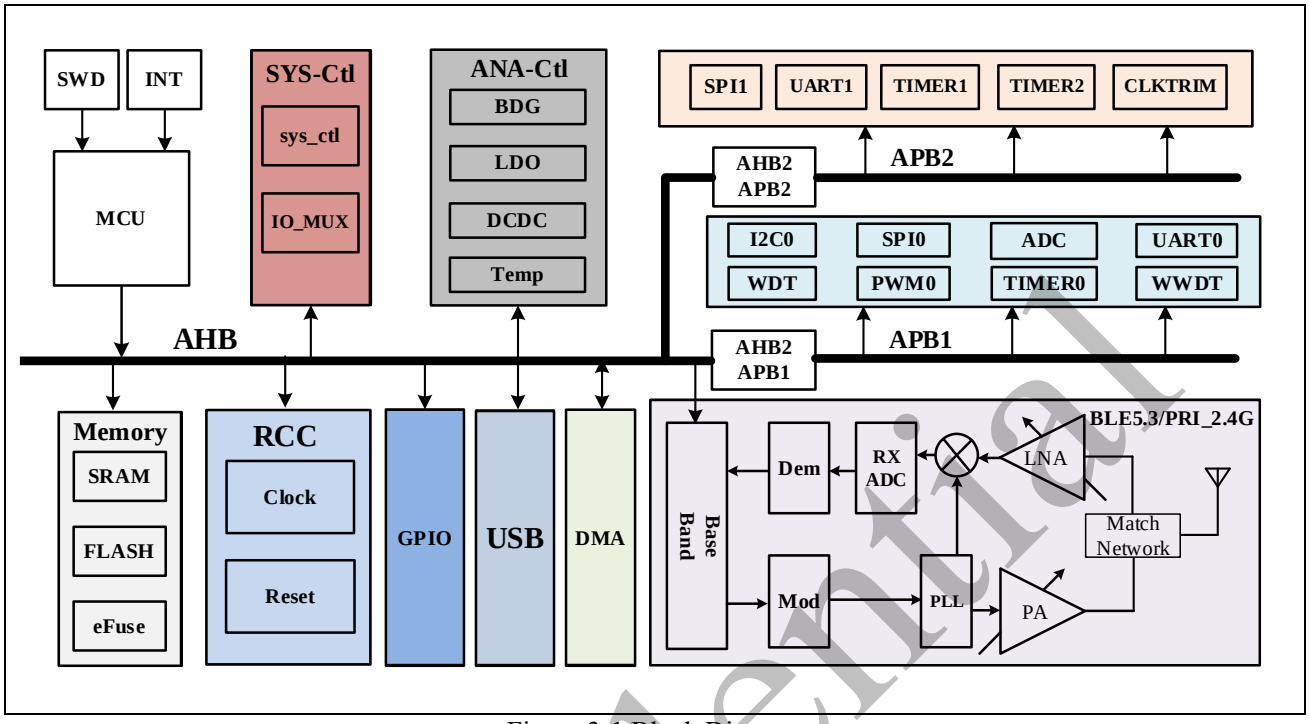


Figure 3-1 Block Diagram

4 Pin Information

4.1 Pin Diagram

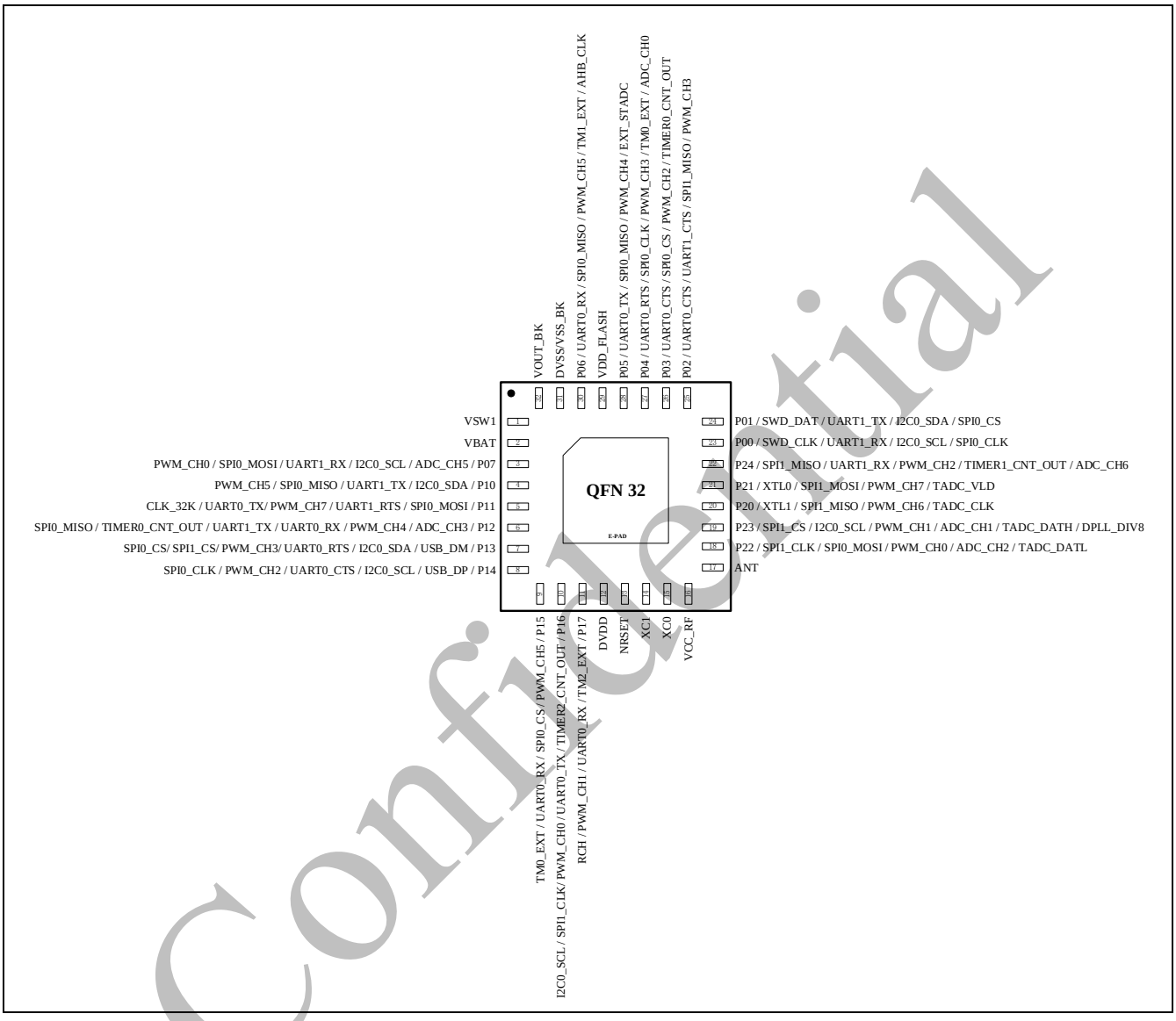


Figure 4-1 QFN 32 Diagram

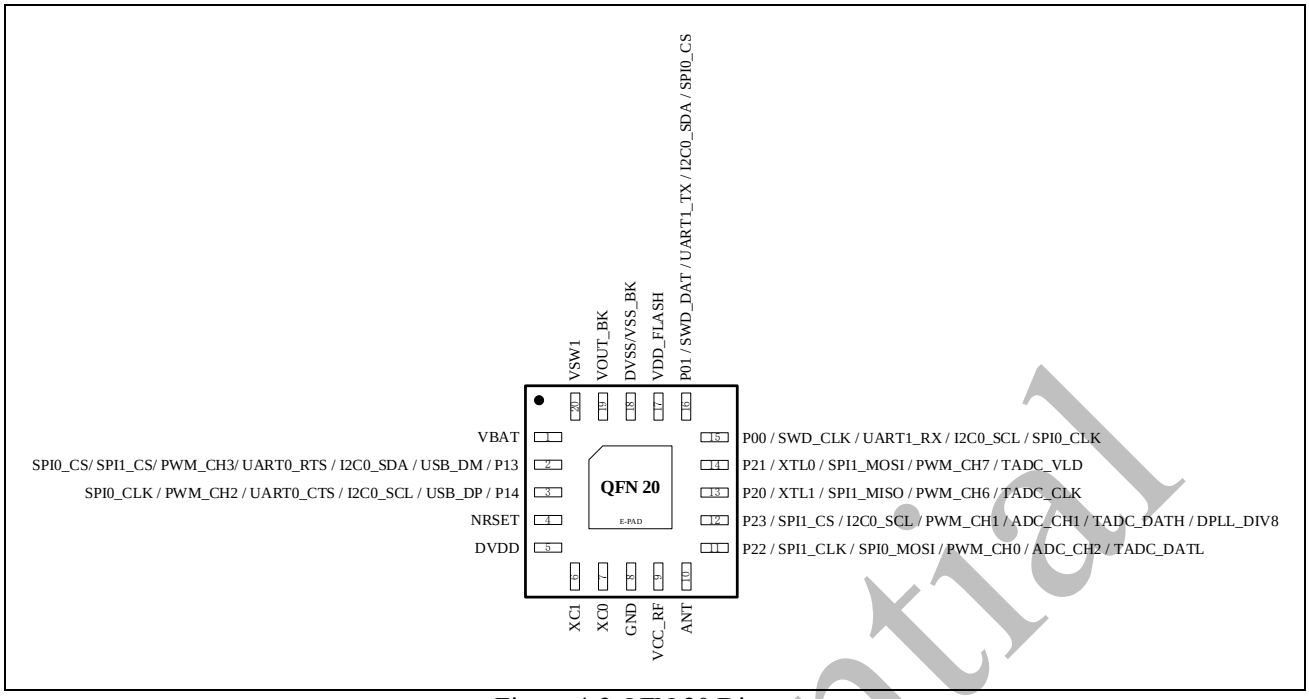


Figure 4-2 QFN 20 Diagram

4.2 Pin Descriptions

Detail pin descriptions see Table 4-1.

Pin No.		Pin Name	Pin Type	Description
QFN32	QFN20			
1	20	VSW1	P	DCDC internal power switch (switching frequency is about 650kHz), an external inductor is required when using
2	1	VBAT	P	Power input
3	-	P07	I/O	General-purpose digital input and output
		UART1_RX	I	Uart1 rx
		I2C0_SCL	I/O	I2c0 scl
		SPI0_MOSI	I/O	Spi0 mosi
		PWM_CH0	O	Channel 0 PWM output
		ADC_CH5	AI	Channel 5 ADC input
4	-	P10	I/O	General-purpose digital input and output
		UART1_TX	O	Uart1 tx
		I2C0_SDA	I/O	I2c0 sda
		SPI0_MISO	I/O	Spi0 miso
		PWM_CH5	O	Channel 5 PWM output
5	-	P11	I/O	General-purpose digital input and output
		UART1_RTS	O	Uart1 rts
		SPI0_MOSI	I/O	Spi0 mosi
		PWM_CH7	O	Channel 7 PWM output
		CLK_32K	O	Clk_32k output
		UART0_TX	O	Uart0 tx
6	-	P12	I/O	General-purpose digital input and output
		UART0_RX	I	Uart0 rx
		TIMER0_CNT_OUT	O	Timer0 output
		UART1_TX	O	Uart1 tx
		SPI0_MISO	I/O	Spi0 miso
		PWM_CH4	O	Channel 4 PWM output
		ADC_CH3	AI	Channel 3 ADC input
7	2	P13	I/O	General-purpose digital input and output
		UART0_RTS	O	Uart0 rts

		I2C0_SDA	I/O	I2c0 sda
		PWM_CH3	O	Channel 3 PWM output
		SPI1_CS	I/O	Spi1 cs
		SPI0_CS	I/O	Spi0 cs
		USB_DM	AI/AO	Usb dm
8	3	P14	I/O	General-purpose digital input and output
		UART0_CTS	I	Uart0 cts
		I2C0_SCL	I/O	I2c0 scl
		PWM_CH2	O	Channel 2 PWM output
		SPI0_CLK	I/O	Spi0 clock
		USB_DP	AI/AO	Usb dp
9	-	P15	I/O	General-purpose digital input and output
		SPI0_CS	I/O	Spi0 cs
		PWM_CH5	O	Channel 5 PWM output
		TM0_EXT	I	Timer0 external input
		UART0_RX	I	Uart0 rx
10	-	P16	I/O	General-purpose digital input and output
		UART0_TX	O	Uart0 tx
		PWM_CH0	O	Channel 0 PWM output
		SPI1_CLK	I/O	Spi1 clock
		I2C0_SCL	I/O	I2c0 scl
		TIMER2_CNT_OUT	O	Timer2 output
11	-	P17	I/O	General-purpose digital input and output
		UART0_RX	I	Uart0 rx
		TM2_EXT	I	Timer2 external input
		PWM_CH1	O	Channel 1 PWM output
		RCH	O	Rch output
12	5	DVDD	P	Hldo output , typical value 1.2V
13	4	NRSET	I	Reset pin
14	6	XC1	AO	External 32MHz clock source output
15	7	XC0	AI	External 32MHz clock source input
-	8	GND	P	Ground
16	9	VCC_RF	P	RF power input, can be directly connected to VOUT_BK

17	10	ANT	AI/AO	RF antenna , an external antenna is required for use
18	11	P22	I/O	General-purpose digital input and output
		SPI1_CLK	I/O	Spi1 clock
		PWM_CH0	O	Channel 0 PWM output
		TADC_DATL	O	Tadc_datl output
		SPI0_MOSI	I/O	Spi0 mosi
		ADC_CH2	AI	Channel 2 ADC input
19	12	P23	I/O	General-purpose digital input and output
		SPI1_CS	I/O	Spi1 cs
		PWM_CH1	O	Channel 1 PWM output
		DPLL_DIV8	O	Dpll_div8 output
		TADC_DATH	O	Tadc_dath output
		I2C0_SCL	I/O	I2c0 scl
		ADC_CH1	AI	Channel 1 ADC input
20	13	P20	I/O	General-purpose digital input and output
		XTL1	AO	External 32.768kHz clock source output
		SPI1_MISO	I/O	Spi1 miso
		PWM_CH6	O	Channel 6 PWM output
		TADC_CLK	O	Tadc_clk output
21	14	P21	I/O	General-purpose digital input and output
		XTL0	AI	External 32.768kHz clock source input
		SPI1_MOSI	I/O	Spi1 mosi
		PWM_CH7	O	Channel 7 PWM output
		TADC_VLD	O	Tadc_vld output
22	-	P24	I/O	General-purpose digital input and output
		UART1_RX	I	Uart1 rx
		SPI1_MISO	I/O	Spi1 miso
		PWM_CH2	O	Channel 2 PWM output
		TIMER1_CNT_OUT	O	Timer1 output
		ADC_CH6	AI	Channel 6 ADC input
23	15	P00	I/O	General-purpose digital input and output
		SWD_CLK	I	Swd clock input
		UART1_RX	I	Uart1 rx

		I2C0_SCL	I/O	I2c0 scl
		SPI0_CLK	I/O	Spi0 clock
24	16	P01	I/O	General-purpose digital input and output
		SWD_DAT	I/O	Swd data input and output
		UART1_TX	O	Uart1 tx
		I2C0_SDA	I/O	I2c0 sda
		SPI0_CS	I/O	Spi0 cs
25	-	P02	I/O	General-purpose digital input and output
		UART0_CTS	I	Uart0 cts
		SPI1_MISO	I/O	Spi1 miso
		PWM_CH3	O	Channel 3 PWM output
		UART1_CTS	I	Uart1 cts
26	-	P03	I/O	General-purpose digital input and output
		UART0_CTS	I	Uart0 cts
		SPI0_CS	I/O	Spi0 cs
		PWM_CH2	O	Channel 2 PWM output
		TIMER0_CNT_OUT	O	Timer0 output
27	-	P04	I/O	General-purpose digital input and output
		UART0_RTS	O	Uart0 rts
		SPI0_CLK	I/O	Spi0 clock
		PWM_CH3	O	Channel 3 PWM output
		TM0_EXT	I	Timer0 external input
		ADC_CH0	AI	Channel 0 ADC input
28	-	P05	I/O	General-purpose digital input and output
		UART0_TX	O	Uart0 tx
		SPI0_MISO	I/O	Spi0 miso
		PWM_CH4	O	Channel 4 PWM output
		EXT_STADC	I	Ext_stadc input
29	17	VDD_FLASH	P	FLASH power input
30	-	P06	I/O	General-purpose digital input and output
		UART0_RX	I	Uart0 rx
		SPI0_MISO	I/O	Spi0 miso
		PWM_CH5	O	Channel 5 PWM output

		TM1_EXT	I	Timer1 external input
		AHB_CLK	O	Ahb_clk output
31	18	DVSS/VSS_BK	P	Common ground terminal of DCDC power supply, independent power ground
32	19	VOUT_BK	P	DCDC voltage output
33	21	E-PAD	P	Chip bottom pad, common ground

Table 4-1 Pin Descriptions

5 Electrical specification

Maximum and minimum values

In the notes below each table, the data obtained through comprehensive evaluation, design simulation and/or process features are not tested on the production line; based on the comprehensive evaluation, the minimum and maximum values are after the sample test. Take the average value and add and subtract three times the standard distribution (average ± 3 Σ).

5.1 RF characteristics

Table 5-1 RF characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{OP}	Operating frequency		2400	-	2483	MHz
PLLres	PLL programming resolution		244	1M	-	Hz
DR	Data rate		0.125	-	2	Mbps
$\Delta f_{BLE,2M}$	Frequency deviation @ BLE 2Mbps		450	500	550	kHz
$\Delta f_{BLE,1M}$	Frequency deviation @ BLE 1Mbps		225	250	275	kHz
$\Delta f_{297,2M}$	Frequency deviation @ 297mode 2Mbps		450	500	550	kHz
$\Delta f_{297,1M}$	Frequency deviation @ 297mode 1Mbps		225	250	275	kHz
$\Delta f_{N,2M}$	Frequency deviation @ N-mode 2Mbps		-	320	-	kHz
$\Delta f_{N,1M}$	Frequency deviation @ N-mode 1Mbps		-	170	-	kHz
$\Delta f_{BLE,2M}$	Channel spacing @ BLE 2Mbps		-	2	-	MHz
$\Delta f_{BLE,1M}$	Channel spacing @ BLE 1Mbps		-	2	-	MHz
$\Delta f_{297,2M}$	Channel spacing @ 297mode 2Mbps		-	2	-	MHz
$\Delta f_{297,1M}$	Channel spacing @ 297mode 1Mbps		-	1	-	MHz
$\Delta f_{N,2M}$	Channel spacing @ N-mode 2Mbps		-	2	-	MHz
$\Delta f_{N,1M}$	Channel spacing @ N-mode 1Mbps		-	1	-	MHz

Table 5-2 TX characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
P_{RFTX}	Output power		-	-	9	dBm
P_{RFC}	RF power control range		-	40	-	dB
P_{RFCR}	RF power accuracy		-	-	±3	dB
$P_{RF1M,1}$	1st Adjacent Channel Transmit Power @1Mbps		-	-40	-	dBc
$P_{RF1M,2}$	2nd Adjacent Channel Transmit Power @1Mbps		-	-56	-	dBc
$P_{RF1M,\geq 3}$	3rd Adjacent Channel Transmit Power @1Mbps		-	-60	-	dBc

$P_{RF2M,2}$	1st Adjacent Channel Transmit Power @2Mbps		-	-37	-	dBc
$P_{RF2M,4}$	2nd Adjacent Channel Transmit Power @2Mbps		-	-58	-	dBc
$P_{RF2M,\geqslant 6M}$	3rd Adjacent Channel Transmit Power @2Mbps		-	-60	-	dBc
P_{BW1M}	20dB bandwidth @1Mbps		-	1.3	-	MHz
P_{BW2M}	20dB bandwidth @2Mbps		-	2.3	-	MHz
$P_{SP,1}$	Spurious @≤1GHz		-	-	-73	dBm
$P_{SP,2}$	Spurious @≥1GHz		-	-	-49	dBm

Table 5-3 RX characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$P_{RX,MIX}$	Receive maximum input power		-	0	-	dBm
$P_{SENS,1M,BLE}$	Sensitivity, 1Mbps BLE		-	-96	-	dBm
$P_{SENS,2M,BLE}$	Sensitivity, 2Mbps BLE		-	-93	-	dBm
$P_{SENS,125K,BLE}$	Sensitivity, 125kbps BLE		-	-99	-	dBm
$P_{SENS,500K,BLE}$	Sensitivity, 500kbps BLE		-	-99	-	dBm
$P_{SENS,250K,B}$	Sensitivity, 250kbps B mode	Sensitivity, 1Mbps ideal transmitter, ≤37 bytes, BER = 0.1% is presented.	-	-99	-	dBm
$P_{SENS,1M,297}$	Sensitivity, 1Mbps 297 mode		-	-93	-	dBm
$P_{SENS,2M,297}$	Sensitivity, 2Mbps 297 mode		-	-91	-	dBm
$P_{SENS,250K,297}$	Sensitivity, 250kbps 297 mode		-	-99	-	dBm
$P_{SENS,1M,N}$	Sensitivity, 1Mbps N-mode		-	-93	-	dBm
$P_{SENS,2M,N}$	Sensitivity, 2Mbps N-mode		-	-91	-	dBm
$P_{SENS,250K,N}$	Sensitivity, 250kbps N-mode		-	-99	-	dBm
$C/I_{CO,1M,BLE}$	Co-Channel interference@1Mbps		-	6	-	dB
$C/I_{1M,1M,BLE}$	Adjacent (1 MHz) interference@1Mbps		-	-3	-	dB
$C/I_{2M,1M,BLE}$	Adjacent (2 MHz) interference @1Mbps		-	-40	-	dB
$C/I_{\geq 3M,1M,BLE}$	Adjacent (≥3 MHz) interference @1Mbps		-	-45	-	dB
$C/I_{Image,1M,BLE}$	Image frequency interference @1Mbps		-	-23	-	dB
$C/I_{Image\pm 1M,1M,BLE}$	Adjacent (±1MHz) interference to in-band image frequency @1Mbps		-	-38	-	dB
$C/I_{\geq 6M,1M,BLE}$	Adjacent (≥6 MHz) interference @1Mbps		-	-45	-	dB
$C/I_{CO,2M,BLE}$	Co-Channel interference @2Mbps		-	7	-	dB
$C/I_{2M,2M,BLE}$	Adjacent (2 MHz) interference @2Mbps		-	-3	-	dB
$C/I_{4M,2M,BLE}$	Adjacent (4 MHz) interference @2Mbps		-	-37	-	dB

$C/I_{\geq 6M,2M,BLE}$	Adjacent (≥6 MHz) interference @2Mbps		-	-35	-	dB
$C/I_{Image,2M,BLE}$	Image frequency interference @2Mbps		-	-23	-	dB
$C/I_{Image\pm 2M,2M,BLE}$	Adjacent (±2 MHz) interference to in-band image frequency		-	-36	-	dB
$C/I_{\geq 12M,2M,BLE}$	Adjacent (≥12 MHz) interference @2Mbps		-	-35	-	dB
$C/I_{CO,125K,BLE}$	Co-Channel interference @125kbps		-	-6	-	dB
$C/I_{1M,125K,BLE}$	Adjacent (1 MHz) interference @125kbps		-	-13	-	dB
$C/I_{2M,125K,BLE}$	Adjacent (2 MHz) interference @125kbps		-	-37	-	dB
$C/I_{\geq 3M,125K,BLE}$	Adjacent (≥3MHz) interference @125kbps		-	-49	-	dB
$C/I_{Image,125K,BLE}$	Image frequency interference @125kbps		-	-31	-	dB
$C/I_{Image\pm 1M,125K,BLE}$	Adjacent (±1MHz) interference to in-band image frequency @125kbps		-	-48	-	dB
$C/I_{CO,500K,BLE}$	Co-Channel interference @500kbps		-	1	-	dB
$C/I_{1M,500K,BLE}$	Adjacent (1 MHz) interference @500kbps		-	-6	-	dB
$C/I_{2M,500K,BLE}$	Adjacent (2 MHz) interference @500kbps		-	-31	-	dB
$C/I_{\geqslant 3M,500K,BLE}$	Adjacent (≥3MHz) interference @500kbps		-	-43	-	dB
$C/I_{Image,500K,BLE}$	Image frequency interference @500kbps		-	-25	-	dB
$C/I_{Image\pm 1M,500K,BLE}$	Adjacent (±1MHz) interference to in-band image frequency @500kbps		-	-41	-	dB
$C/I_{CO,1M,297}$	Co-Channel interference @1Mbps		-	TBD	-	dB
$C/I_{1M,1M,297}$	Adjacent (1 MHz) interference @1Mbps		-	TBD	-	dB
$C/I_{2M,1M,297}$	Adjacent (2 MHz) interference @1Mbps		-	TBD	-	dB
$C/I_{\geqslant 3M,1M,297}$	Adjacent (≥3 MHz) interference @1Mbps		-	TBD	-	dB
$C/I_{Image,1M,297}$	Image frequency interference @1Mbps		-	TBD	-	dB
$C/I_{Image\pm 1M,1M,297}$	Adjacent (±1MHz) interference to in-band image frequency @1Mbps		-	TBD	-	dB
$C/I_{\geqslant 6M,1M,297}$	Adjacent (≥6 MHz) interference @1Mbps		-	TBD	-	dB
$C/I_{CO,2M,297}$	Co-Channel interference @2Mbps		-	TBD	-	dB
$C/I_{2M,2M,297}$	Adjacent (2 MHz) interference @2Mbps		-	TBD	-	dB
$C/I_{4M,2M,297}$	Adjacent (4 MHz) interference @2Mbps		-	TBD	-	dB
$C/I_{\geq 6M,2M,297}$	Adjacent (≥6 MHz) interference @2Mbps		-	TBD	-	dB
$C/I_{Image,2M,297}$	Image frequency interference @2Mbps		-	TBD	-	dB
$C/I_{Image\pm 2M,2M,297}$	Adjacent (±2MHz) interference to in-band image frequency @2Mbps		-	TBD	-	dB
$C/I_{\geqslant 12M,2M,297}$	Adjacent (≥12 MHz) interference @2Mbps		-	TBD	-	dB
$C/I_{CO,250K,297}$	Co-Channel interference @250kbps		-	TBD	-	dB

$C/I_{1M,250K,297}$	Adjacent (1 MHz) interference @250kbps		-	TBD	-	dB
$C/I_{2M,250K,297}$	Adjacent (2 MHz) interference @250kbps		-	TBD	-	dB
$C/I_{\geqslant 3M,250K,297}$	Adjacent (≥3MHz) interference @250kbps		-	TBD	-	dB
$C/I_{Image,250K,297}$	Image frequency interference @250kbps		-	TBD	-	dB
$C/I_{Image\pm 1M,250K,297}$	Adjacent (±1MHz) interference to in-band image frequency @250kbps		-	TBD	-	dB
$C/I_{CO,1M,N}$	Co-Channel interference@1Mbps		-	TBD	-	dB
$C/I_{1M,1M,N}$	Adjacent (1 MHz) interference@1Mbps		-	TBD	-	dB
$C/I_{2M,1M,N}$	Adjacent (2 MHz) interference @1Mbps		-	TBD	-	dB
$C/I_{\geqslant 3M,1M,N}$	Adjacent (≥3 MHz) interference @1Mbps		-	TBD	-	dB
$C/I_{Image,1M,N}$	Image frequency interference@1Mbps		-	TBD	-	dB
$C/I_{Image\pm 1M,1M,N}$	Adjacent (±1MHz) interference to in-band image frequency @1Mbps		-	TBD	-	dB
$C/I_{\geqslant 6M,1M,N}$	Adjacent (≥6 MHz) interference @1Mbps		-	TBD	-	dB
$C/I_{CO,2M,N}$	Co-Channel interference @2Mbps		-	TBD	-	dB
$C/I_{2M,2M,N}$	Adjacent (2 MHz) interference @2Mbps		-	TBD	-	dB
$C/I_{4M,2M,N}$	Adjacent (4 MHz) interference @2Mbps		-	TBD	-	dB
$C/I_{\geq 6M,2M,N}$	Adjacent (≥6 MHz) interference @2Mbps		-	TBD	-	dB
$C/I_{Image,2M,N}$	Image frequency interference @2Mbps		-	TBD	-	dB
$C/I_{Image\pm 2M,2M,N}$	Adjacent (±2 MHz) interference to in-band image frequency @2Mbps		-	TBD	-	dB
$C/I_{\geqslant 12M,2M,N}$	Adjacent (≥12 MHz) interference @2Mbps		-	TBD	-	dB
$C/I_{CO,250K,N}$	Co-Channel interference @250kbps		-	TBD	-	dB
$C/I_{1M,250K,N}$	Adjacent (1 MHz) interference @250kbps		-	TBD	-	dB
$C/I_{2M,250K,N}$	Adjacent (2 MHz) interference @250kbps		-	TBD	-	dB
$C/I_{\geqslant 3M,250K,N}$	Adjacent (≥3MHz) interference @250kbps		-	TBD	-	dB
$C/I_{Image,250K,N}$	Image frequency interference @250kbps		-	TBD	-	dB
$C/I_{Image\pm 1M,250K,N}$	Adjacent (±1MHz) interference to in-band image frequency @250kbps		-	TBD	-	dB
$C/I_{CO,250K,B}$	Co-Channel interference @250kbps		-	TBD	-	dB
$C/I_{1M,250K,B}$	Adjacent (1MHz) interference @250kbps		-	TBD	-	dB
$C/I_{2M,250K,B}$	Adjacent (2MHz) interference @250kbps		-	TBD	-	dB
$C/I_{\geqslant 3M,250K,B}$	Adjacent (≥3MHz) interference @250kbps		-	TBD	-	dB
$C/I_{Image,250K,B}$	Image frequency interference @250kbps		-	TBD	-	dB
$C/I_{Image\pm 1M,250K,B}$	Adjacent (±1MHz) interference to in-band image frequency @250kbps		-	TBD	-	dB

$P_{IMD,5TH,1M}$	IMD performance 5 MHz offset @1Mbps		-	TBD	-	dBm
$P_{IMD,5TH,2M}$	IMD performance 10 MHz offset @2Mbps		-	TBD	-	dBm

Table 5-4 RSSI characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$RSSI_{RFC}$	RSSI indication range		-90	-	-15	dBm
$RSSI_{Auu}$	RSSI accuracy		-	±2	-	dB
$RSSI_{Res}$	RSSI resolution		-	0.25	-	dB
$RSSI_{Per}$	RSSI Sample period		-	0.25	-	us

Table 5-5 RF Timing characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$T_{OSC,EN}$	Crystal oscillator settling time		-	TBD	-	us
$T_{TX,EN}$	Time between TXEN task and READY event after channel FREQUENCY configured		-	TBD	-	us
$T_{RX,EN}$	Time between the RXEN task and READY event after channel FREQUENCY configured in default mode		-	TBD	-	us
$T_{TX,DISABLE}$	Time between DISABLE task and DISABLED event when the radio was in TX		-	TBD	-	us
$T_{RX,DISABLE}$	Time between DISABLE task and DISABLED event when the radio was in RX		-	TBD	-	us
T_{RX-TX}	The time taken to switch from RX to TX or TX to RX		-	150	-	us

Table 5-6 RF power characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$I_{TX,P9dBm,DCDC}$	TX only run current 9dBm @DC-DC		-	13.97	-	mA
$I_{TX,P6dBm,DCDC}$	TX only run current 6dBm @DC-DC		-	9.59	-	mA
$I_{TX,P4dBm,DCDC}$	TX only run current 4dBm @DC-DC		-	6.67	-	mA
$I_{TX,P0dBm,DCDC}$	TX only run current 0dBm @DC-DC		-	5.06	-	mA
$I_{TX,P-4dBm,DCDC}$	TX only run current -4dBm @DC-DC		-	2.56	-	mA
$I_{TX,P-8dBm,DCDC}$	TX only run current -8dBm @DC-DC		-	2.15	-	mA
$I_{TX,P-12dBm,DCDC}$	TX only run current -12dBm @DC-DC		-	1.87	-	mA
$I_{TX,P-16dBm,DCDC}$	TX only run current -16dBm @DC-DC		-	1.64	-	mA
$I_{TX,P-20dBm,DCDC}$	TX only run current -20dBm @DC-DC		-	1.53	-	mA

$I_{TX,P-40dBm,DCDC}$	TX only run current -40dBm @DC-DC		-	1.12	-	mA
$I_{TX,P9dBm,LDO}$	TX only run current 9dBm @LDO		-	35.55	-	mA
$I_{TX,P6dBm,LDO}$	TX only run current 6dBm @LDO		-	16.28	-	mA
$I_{TX,P4dBm,LDO}$	TX only run current 4dBm @LDO		-	12.1	-	mA
$I_{TX,P0dBm,LDO}$	TX only run current 0dBm @LDO		-	9.43	-	mA
$I_{TX,P-4dBm,LDO}$	TX only run current -4dBm @LDO		-	5.74	-	mA
$I_{TX,P-8dBm,LDO}$	TX only run current -8dBm @LDO		-	5.08	-	mA
$I_{TX,P-12dBm,LDO}$	TX only run current -12dBm @LDO		-	4.62	-	mA
$I_{TX,P-16dBm,LDO}$	TX only run current -16dBm @LDO		-	4.04	-	mA
$I_{TX,P-20dBm,LDO}$	TX only run current -20dBm @LDO		-	3.92	-	mA
$I_{TX,P-40dBm,LDO}$	TX only run current -40dBm @LDO		-	3.00	-	mA
$I_{RX,1M,DCDC}$	RX 1Mbps current @DC-DC		-	2.50	-	mA
$I_{RX,2M,DCDC}$	RX 2Mbps current @DC-DC		-	2.71	-	mA
$I_{RX,1M,LDO}$	RX 1Mbps current @LDO		-	4.82	-	mA
$I_{RX,2M,LDO}$	RX 2Mbps current @LDO		-	5.67	-	mA

Test conditions and methods.

1. Transceiver power consumption tested in 1M mode using BLE ADV broadcast mode.
2. 2M mode is used is the power consumption when BLE connection.
3. The power consumption tested is the RF peak power.
4. The test method uses the total power consumption minus the power consumption of the MCU when the RF is not operating to calculate the final power consumption.
5. The sample software tested is based on peripheral_hr.
6. 3.3V Power Supply

5.2 GPIO characteristics

Table 5-7 GPIO characteristics (single IO)

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{IH}	Input high voltage	T_A=25°C	-	-	0.24*VDD	V
V_{IL}	Input low voltage	Load capacitance =20pF, T_A=25°C	-	0.3	-	V
V_{HYS}	Input hysteresis voltage, $V_{hys}=V_{IH}-V_{IL}$	T_A=25°C	-	-	0.24*VDD	V
C_{Iana}	Analog input capacitors	T_A=25°	-	300	-	fF
I_{Lkg}	Leakage current, open-drain mode or input mode	VDD≤VIN≤3.6V	-	-	TBD	uA
R_{PU}	Pull-up resistor	Vin =VSS, VDD =3.3V	-	50	-	kΩ
R_{PD}	Pull-down resistor	Vin =VSS, VDD =3.3V	-	100	-	kΩ

V_I	Input voltage	T_A=25°C	VSS	-	VDD	V
V_O	Output voltage	T_A=25°C	VSS	-	VDD	V
I_{source}	Source current （Push-pull output）（Except for P03, P15）	Vin =VDD-0.5V	8.5	9.5	10.5	mA
	Source current （Push-pull output）（P03, P15）		21	22	23	mA
I_{Sink}	Sink current（Push-pull output）	Vin =VSS+0.5V, T_A=25°C	19.5	20.5	21.5	mA
f_{Port_CLK}	IO output frequency	Load capacitance =20pF	-	-	48	MHz

Table 5-8 Combined test

Description	Conditions	Status	Remark
IO default state after power on	VDD=3.3V ,T_A=25°C	P00, P01: Pull-up input state Others: High resistance state	
IO status in deepsleep mode	VDD=3.3V ,T_A=25°C	Deepsleep: All gpio retention Standby_m1: All gpio retention Standby_m0: P00, P01, P02 retention	
IO status at reset	VDD=3.3V ,T_A=25°C	P00, P01: Pull-up input state Others: High resistance state	

Table 5-9 nRESET Input Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{ILR}	Negative threshold voltage, nRESET	VDD=1.8V-3.3V ,T_A=25°C	-	-	0.22*VDD	V
V_{IHR}	Positive threshold voltage, nRESET	VDD=1.8V-3.3V ,T_A=25°C	0.48*VDD	-	-	V
V_{hys_rst}	Schmitt Trigger Voltage Hysteresis	VDD=1.8V-3.3V ,T_A=25°C	-	-	0.26*VDD	V
R_{RST}	nRESET pin internal pull-up resistor	VDD=3.3V ,T_A=25°C	-	7.5	-	kΩ
$t_{FR,\ 0.3pF}$	nRESET pin input filter pulse time	VDD=3.3V ,T_A=25°C	-	TBD	-	ns

5.3 Reset characteristics

Table 5-10 Reset characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{BOD}	Brown-out detection voltage threshold	BODSEL<2:0> = 000(falling edge)，dVDD/dt≤3V/s	-	1.84	-	V
		BODSEL<2:0> = 001(falling edge)，	-	1.96	-	

		dVDD/dt≤3V/s				
		BODSEL<2:0> = 010(falling edge), dVDD/dt≤3V/s	-	2.05	-	
		BODSEL<2:0> = 011(falling edge), dVDD/dt≤3V/s	-	2.16	-	
		BODSEL<2:0> = 100(falling edge), dVDD/dt≤3V/s	-	2.25	-	
		BODSEL<2:0> = 101(falling edge), dVDD/dt≤3V/s	-	2.35	-	
		BODSEL<2:0> = 110(falling edge), dVDD/dt≤3V/s	-	2.47	-	
V_{BODhys}	BOD hysteresis voltage	dVDD/dt≤3V/s	100	-	160	mV
T_{BOD_RE1}	BOD response Time(Normal mode)	dVDD/dt≤3V/s	1	32	32	Slow clock
I_{BOD}	BOD operating current	dVDD/dt≤3V/s	-	0.5	-	uA
V_{POR}	Power on reset voltage threshold	Rising edge, dvdd/dt≤3V/s	-	1.71	-	V
		Falling edge, dvdd/dt≤3V/s	-	1.69	-	V
T_{POR}	POR settling time	VBAT =3.3V	-	1.12	-	ms
V_{LVR}	LVR detection voltage threshold	Falling edge, dvdd/dt≤3V/s	-	1.85	-	V
T_{LVR_RE}	LVR response time	T_A=25°C, dVDD/dt≤3V/s	1	32	32	Slow clock
I_{LVR}	LVR operating current	T_A=25°C, dVDD/dt≤3V/s	-	0.1	-	uA

5.4 Clock characteristics

Table 5-11 HXTAL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{HXTL}	High speed crystal oscillator (HXTAL) frequency	VDD=3.3V ,T_A=25°C	-	32	-	MHz
$C_{LoadHXTL}$	Crystal load capacitance	VDD=3.3V ,T_A=25°C	7	9	12	pF
I_{DDHXTL}	HXTAL oscillator operating current	VDD=3.3V ,T_A=25°C	-	250	-	μA
t_{SUHXTL}	HXTAL oscillator startup time	VDD=3.3V ,T_A=25°C, ESR=40Ω, C_{HXTL}= 9pF	-	465	-	μs
$t_{SUHXTL\ Quick}$	HXTAL oscillator Quick startup time	VDD=3.3V ,T_A=25°C, ESR=40Ω, C_{HXTL}= 9pF	-	155	-	μs
ESR			-	40	-	Ω
$F_{TOLHXTL}$	Frequency tolerance for the crystal	VDD=3.3V ,T_A=25°C	-20	-	20	ppm
PD_{HXTL}	Drive level	VDD=3.3V ,T_A=25°C	-	-	100	μW

Table 5-12 LXTAL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{LXTL}	Low speed crystal oscillator (LXTAL) frequency	VDD=3.3V ,T_A=25°C	-	32.768	-	kHz
I_{DDLXTL}	LXTAL oscillator operating current	VDD=3.3V ,T_A=25°C	0.3	0.45	0.67	μA
t_{SULXTL}	LXTAL oscillator Normal startup time	VDD=3.3V ,T_A=25°C	330	550	1500	ms
$t_{SULXTL\ Quick}$	LXTAL oscillator Quick startup time	VDD=3.3V ,T_A=25°C	-	125	-	ms
ESR_{LXTL}	Equivalent series resistance 6 pF < CL ≤ 9 pF	VDD=3.3V ,T_A=25°C	-	70	-	kΩ
$C_{LoadLXTL}$	Crystal load capacitance	VDD=3.3V ,T_A=25°C	-	7	-	pF
PD_{LXTL}	Drive level	VDD=3.3V ,T_A=25°C	-	-	1	μW

Table 5-13 32MHz RCH characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{IRC32M}	Crystal frequency	VDD=3.3V ,T_A=25°C	-	32	-	MHz
ACC_{IRC32M}	Frequency accuracy	VDD=3.3V, T_A=-40°C ~+105°C	-	-	-	%
		VDD=3.3V, T_A=-20°C ~ +85°C	-	-	-	%
		VDD=3.3V, T_A=25°C	-	±1	-	%
D_{IRC32M}	IRC32M oscillator duty cycle	VDD=3.3V, f_{IRC}32M=32MHz, T_A=25°C	48	50	52	%
$I_{DDIRC32M}$	Operating current	VDD=3.3V, f_{IRC8M}=32MHz, T_A=25°C	-	82	-	μA
$t_{SUIRC32M}$	Startup time	VDD=3.3V, f_{IRC32M}=32MHz, T_A=25°C	-	5	-	μs
$d_{fIRC32M}$	25°C, the frequency drifts with the supply voltage	VDD=1.8V~3.6V, T_A=25°C	-	0.5	-	%/V

Table 5-14 32kHz RCL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{IRC32k}	Crystal frequency	VDD=3.3V ,T_A=25°C	-	32	-	kHz
ACC_{IRC32K}	Frequency accuracy	VDD=3.3V, T_A=25°C (After calibration）	-	±500	-	ppm
D_{IRC32K}	IRC32K oscillator duty cycle	VDD=3.3V, f_{IRC32K}=32kHz, T_A=25°C	48	50	52	%
$I_{DDIRC32K}$	Operating current	VDD=3.3V, f_{IRC8K}=32kHz, T_A=25°C	-	310	-	nA
$t_{SUIRC32K}$	Startup time	VDD=3.3V, f_{IRC32K}=32kHz,	-	480	-	μs

		T_A=25°C				
df_{IRC32K}	25°C, The frequency drifts with the supply voltage	VDD=1.8V~3.6V, T_A=25°C	-	1	-	%/V

Table 5-15 DPLL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{PLLIN}	PLL input clock frequency	VDD=3.3V, T_A=25°C	-	32	-	MHz
f_{PLL}	PLL output clock frequency	VDD=3.3V, T_A=25°C	48	48	48	MHz
I_{PLL}	Operating current	VDD=3.3V, T_A=25°C	96	105	145	μA

5.5 ADC characteristics

Table 5-16 Power supply and input range conditions

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$V_{Ax(VBG\ adc)}$	Analog input voltage range，VBG（1.2V）	VDD=3.3V, T_A=25°C	0	-	1.2	V
$V_{Ax(VDD)}$	Analog input voltage range，VDD	VDD=3.3V, T_A=25°C	0	-	VDD	V
I_{ADC}	ADC supply current	VDD=3.3V, T_A=25°C Fadc=16MHz	-	0.55	-	mA
C_{sample}	Internal sample and hold capacitors (PAD and PCB capacitors not included)		-	10	-	pF
R_{ADC}	Sampling switch resistance	0V ≤ VAx ≤ VDD	-	300	-	Ω
R_{In}	External input impedance, continuous sampling	0V ≤ VAx ≤ VDD	0.86	-	4734.70	kΩ

Table 5-17 ADC built-in voltage reference

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VBG_{ADC}	Internal 1.2V Reference Voltage	VDD=3.3V, T_A=25°C	1.1	1.2	1.3	V
T_{Coef}	Temperature factor	T_A=-40°C~105°C; VDD=1.8V~3.6V	-	30	-	ppm/°C

Table 5-18 Time parameters

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
F_{ADC}	ADC clock frequency	VDD=3.3V, T_A=25°C	4	16	24	MHz
T_S	Sample time	VDD=3.3V, T_A=25°C	4	1539	8192	$1/F_{adc}$
T_{CONV}	Conversion time	VDD=3.3V, T_A=25°C	32	1580	8298	$1/F_{adc}$

Table 5-19 Linearity parameter

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
INL	Integral linearity error	VDD=3.3V, T_A=25°C	-	-	±3	LSB
DNL	Differential linearity error	VDD=3.3V, T_A=25°C	-	-	±2	LSB
SNR	Signal to Noise Ratio	Fadc = 16MHz Input Clock 250kHz VDD=3.3V, T_A=25°C	-	64.3	-	dB
THD	Total harmonic distortion		-	75	-	dB
SFDR	Spurious-free signal dynamic range		-	77.29	-	dB
ENOB	Effective number of bits		-	10.33	-	Bit

Table 5-20 RIN

ADC significant bit	F_{ADC}(MHz)	Ts(cycles)	Ts(us)	Rinmax(kΩ)
12	32	4	0.125	0.86
12	32	8	0.25	2.01
12	32	32	1	8.95
12	32	64	2	18.20
12	32	128	4	36.69
12	32	8192	256	2367.20
12	16	4	0.25	2.01
12	16	8	0.5	4.32
12	16	32	2	18.20
12	16	64	4	36.69
12	16	128	8	73.68
12	16	8192	512	4734.70

Note: The sampling condition is continuous sampling.

5.6 PMU characteristics

Table 5-21 PMU characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{HLDO}	HLDO output voltage range, external capacitor	VDD=3.3V, T_A=25°C	1.1	1.2	1.4	V
VDD_{PSRR}	Power supply rejection ratio of VDD	VDD=3.3V, T_A=25°C	-15	-	-	dB

5.7 General operating conditions

Table 5-22 General operating conditions

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VDD*	Operating voltage	T_A=25°C	1.8	-	3.6	V
VIPIO2*	Operating voltage	T_A=25°C	1.8	-	3.6	V
T_{ST}	Storage temperature	-	-65	-	150	℃
T_A	Ambient temperature	-	-40	-	125	℃
$T_{J\text{-}QFN32}$	Junction temperature	QFN32 4x4x0.75-P0.4	-40	-	125	℃
$T_{J\text{-}QFN20}$	Junction temperature	QFN20 3x3x0.75-P0.4	-40	-	125	℃
$R_{\theta JA\text{-}QFN32}$	Thermal resistance	QFN32 4x4x0.75-P0.4	-	41	-	℃/W
$R_{\theta JA\text{-}QFN20}$	Thermal resistance	QFN20 3x3x0.75-P0.4	-	-	-	℃/W

Note: DCDC-OFF

5.8 DCDC characteristics

Table 5-23 DCDC characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{IN_DCDC}	Input voltage range	VDD=3.3V, T_A=25°C	2	-	3.6	V
V_{OUT_DCDC}	Output voltage range	VDD=3.3V, T_A=25°C	1.2	1.5	2	V
T_{EN_DCDC}	Standup time	VDD=3.3V , I_{LOAD}=10mA, T_A=25°C, L_{DCR}=80mΩ	-	200	-	us
η	Efficiency	VDD=3.3V , I_{LOAD}=10mA, T_A=25°C, L_{DCR}=80mΩ	-	88	-	%
$VRPL_{DCDC}$	Ripple	VDD=3.3V, T_A=25°C	-	43	-	mv
I_{OUT}	Drive peak current	VDD=3.3V, T_A=25°C	-	100	-	mA
I_{AVG}	Drive average current	VDD=3.3V, T_A=25°C	-	30	-	mA
L_{DCDC}	Effective inductance	VDD=3.3V, T_A=25°C	-	2.2	-	μH
C_{OUT_DCDC}	Effective load capacitance	VDD=3.3V, T_A=25°C	1	4.7	-	μF
F_{osc_DCDC}	Oscillation frequency	VDD=3.3V, T_A=25°C	-	-	1000	kHz

5.9 ESD characteristics

Table 5-24 ESD characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VESDHBM[1]	ESD @ Human Body Mode	T_A=25°C	-	±4	-	kV
VESDCDM[2]	ESD @ Charge Device Mode	T_A=25°C	-	±2000	-	V
VESDMM[3]	ESD @ machine Mode	T_A=25°C	-	±200	-	V
$I_{latchup}$[4]	Latch up current	T_A=25°C	-	±500	-	mA

Notes:

1. Determined by ANSI/ESDA/JEDEC JS-001 standard, Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) - Device Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 Electrostatic Discharge Sensitivity (ESD) Test Standard.
3. Determined according to JESD22-A115-C electrostatic discharge sensitivity (ESD) test standard.
4. Determined according to JEDEC EIA/JESD78 standard.

5.10 Absolute maximum ratings

Table 5-25 Absolute maximum ratings

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VDD - VSS	Supply voltages	T_A=25°C	-0.3	-	3.6	V
VIN	I/O pin voltage	T_A=25°C	VSS-0.3	-	VDD + 0.3	V
PVDD	Extreme power consumption	VDD=3.3V, T_A=25°C DCDC power supply	-	-	TBD	mW

5.11 MCU current characteristics

Symbol	Parameter	Conditions		DCDC OFF	DCDC ON
				Typ(mA)	Typ(mA)
Run mode	All peripherals clock on, run while(1) in flash	System clock source: RCH (.cal 32M)	4M	0.91	0.686
			8M	1.3	0.916
			16M	2.09	1.36
			32M	3.77	2.28
		System clock source: XTH (.off rch)	4M	1.42	0.985
			8M	1.81	1.2
			16M	2.61	1.64
			32M	4.29	2.54
		System clock source: DPLL	6M	1.56	1.05
			12M	2.15	1.38

		(.ref rch(.cal 32M)) (.base 48M)	24M	3.4	2.05
			48M	5.71	3.44
		System clock source： DPLL (.ref xth) (.base 48M) (.off rch)	6M	2.08	1.34
			12M	2.69	1.67
			24M	3.95	2.34
			48M	6.18	3.57
		System clock source： DPLL (.ref rch(.cal 32M)) (.base 64M)	4M	1.39	0.953
			8M	1.78	1.17
			16M	2.58	1.61
			32M	4.27	2.51
		System clock source： DPLL (.ref xth) (.base 64M) (.off rch)	4M	1.9	1.25
			8M	2.3	1.46
			16M	3.13	1.91
			32M	4.85	2.82
	All peripherals clock off, run while(1) in flash	System clock source： RCH (.cal 32M)	4M	0.736	0.523
			8M	0.943	0.719
			16M	1.37	0.963
			32M	2.23	1.43
		System clock source： XTH (.off rch)	4M	0.945	0.723
			8M	1.15	0.84
			16M	1.57	1.07
			32M	2.42	1.54
		System clock source： DPLL (.ref rch(.cal 32M)) (.base 48M)	6M	1.01	0.747
			12M	1.32	0.921
			24M	1.96	1.25
			48M	3.29	2.00
		System clock source： DPLL (.ref xth) (.base 48M) (.off rch)	6M	1.22	0.903
			12M	1.54	1.05
			24M	2.19	1.41
			48M	3.54	2.12
		System clock source： DPLL (.ref rch(.cal 32M)) (.base 64M)	4M	0.925	0.693
			8M	1.14	0.818
			16M	1.56	1.05
			32M	2.43	1.53
		System clock source： DPLL (.ref xth) (.base 64M) (.off rch)	4M	1.14	0.831
			8M	1.35	0.947
			16M	1.78	1.18
			32M	2.66	1.66

Notes: Test conditions - DVDD=1.2V, VDD=3.3V, VBG=1.2V, T_A=25°C

Symbol	**Parameter**	**Conditions**		**Typ(μA)**
standby m0	wake by gpio			0.28
Symbol	**Parameter**	**Conditions**	**Clk source**	**Typ(μA)**
standby m1	wake by 32k timer	sw=0x0d（Note 1）	XTL	1.78(Note 3)

		sw=0x1f（Note 1）	XTL	2.08(Note 3)
	wake by gpio	sw=0x0d（Note 1）		1.22(Note 3)
		sw=0x1f（Note 1）		1.53(Note 3)
	wake by wdt	sw=0x0d（Note 1）	XTL	1.75(Note 3)
		sw=0x1f（Note 1）	XTL	2.08(Note 3)
	wake by lvr	sw=0x0d（Note 1）		1.95(Note 3)
		sw=0x1f（Note 1）		2.32(Note 3)
	wake by bod	sw=0x0d（Note 1）		2.01(Note 3)
		sw=0x1f（Note 1）		2.38(Note 3)
Deepsleep	wake by 32k timer	sw=0x0d（Note 1）	XTL	2.96(Note 3)
		sw=0x1f（Note 1）	XTL	3.37(Note 3)
	wake by gpio	sw=0x0d（Note 1）		2.46(Note 3)
		sw=0x1f（Note 1）		2.86(Note 3)
	wake by wdt	sw=0x0d（Note 1）	XTL	2.99(Note 3)
		sw=0x1f（Note 1）	XTL	3.37(Note 3)
	wake by peripheral timer	sw=0x0d（Note 1）	XTL	4.03(Note 3&4)
		sw=0x1f（Note 1）	XTL	4.73(Note 3)
	wake by 32k timer	sw=0x0d（Note 1）	XTL*	4.06(Note 3&4)
		sw=0x1f（Note 1）	XTL*	4.69(Note 3)
Sleep	wake by gpio	LDO all peripheral clocks on		4620
		LDO non-essential peripheral clocks off		1820
		DCDC all peripheral clocks on		2700
		DCDC non-essential peripheral clocks off		1210

Note: Test conditions - DVDD=1.2V, VDD=3.3V, VBG=1.2V, TA=25°C, DCDC ON

Note*: PWM output enable.

Notes:

1. The ***sw*** indicates the module control switch for PAN107x power retention in low-power mode, bit 1 for power retention, bit 0 for power down, 0d = sram32k+phy_sram+cpu_retention,1f = all_sram_retention
2. In LPLDOH Enhance mode, the lplddoh voltage is affected by lpldoh trim and vref trim, where vref trim compensates ldldoh when ldldoh jitter, so that it does not fall to the voltage of vref trim as much as possible.
3. In LPLDOH mode2, the lpldoh trim voltage does not take effect, and the effective voltage is the vref_trim voltage. The lpldoh undershoot does not occur in this mode, and the bottom current is reduced.
4. PWM can output waveforms normally in *Deepsleep* mode, but only in *Deepsleep* mode2, and see Note 5 for instructions on *Deepsleep* mode2.
5. When the register *LP_FL_CTRL [31]* is 1, the switch between LPLDOL and LPLDOH is connected, and LPLDOL enable is off. LPLDOH supplies power to LPLDOL. This is the mode 2. Mode 2 power consumption increases.

6 Application Reference Diagram

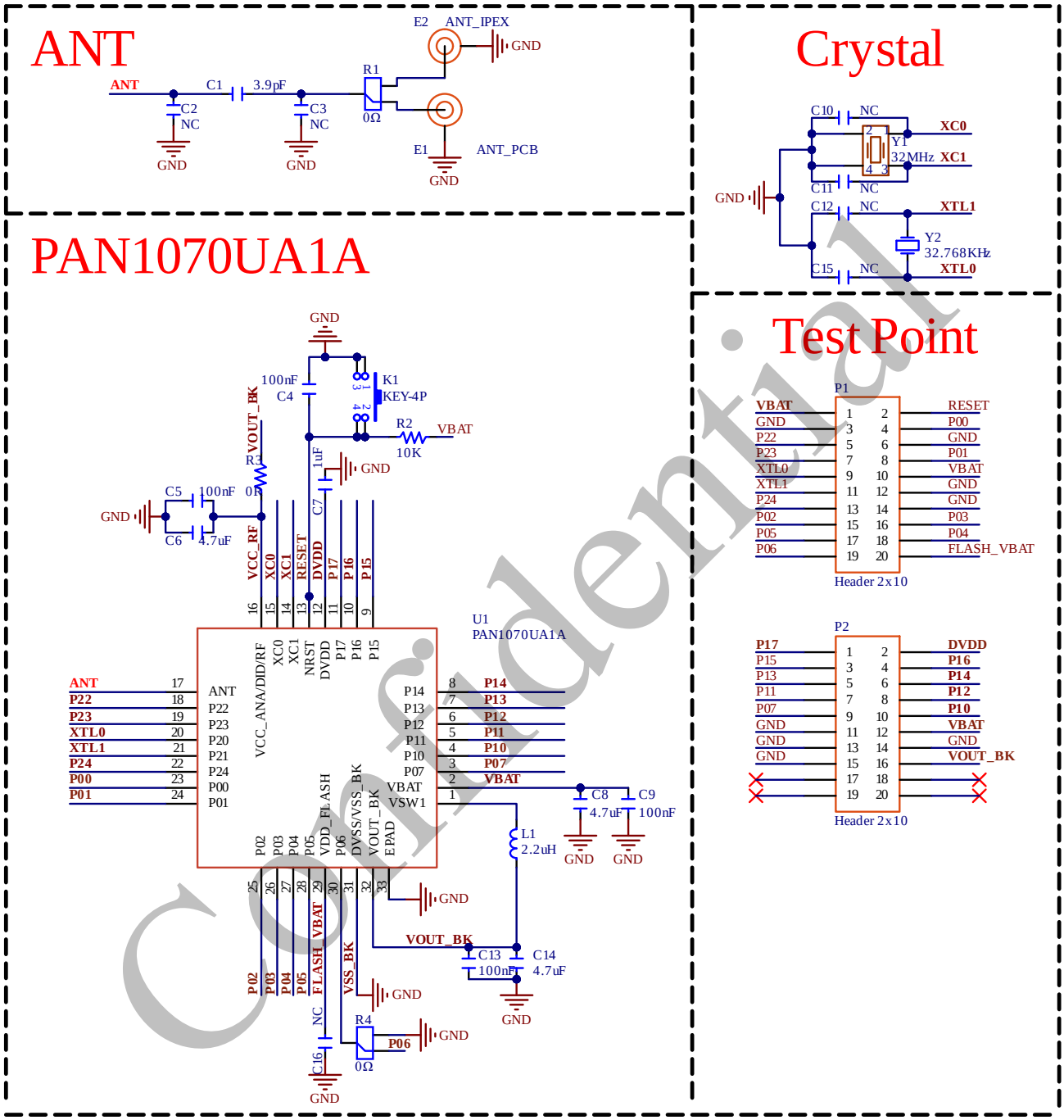


Figure 6-1 Application Schematic of the QFN32

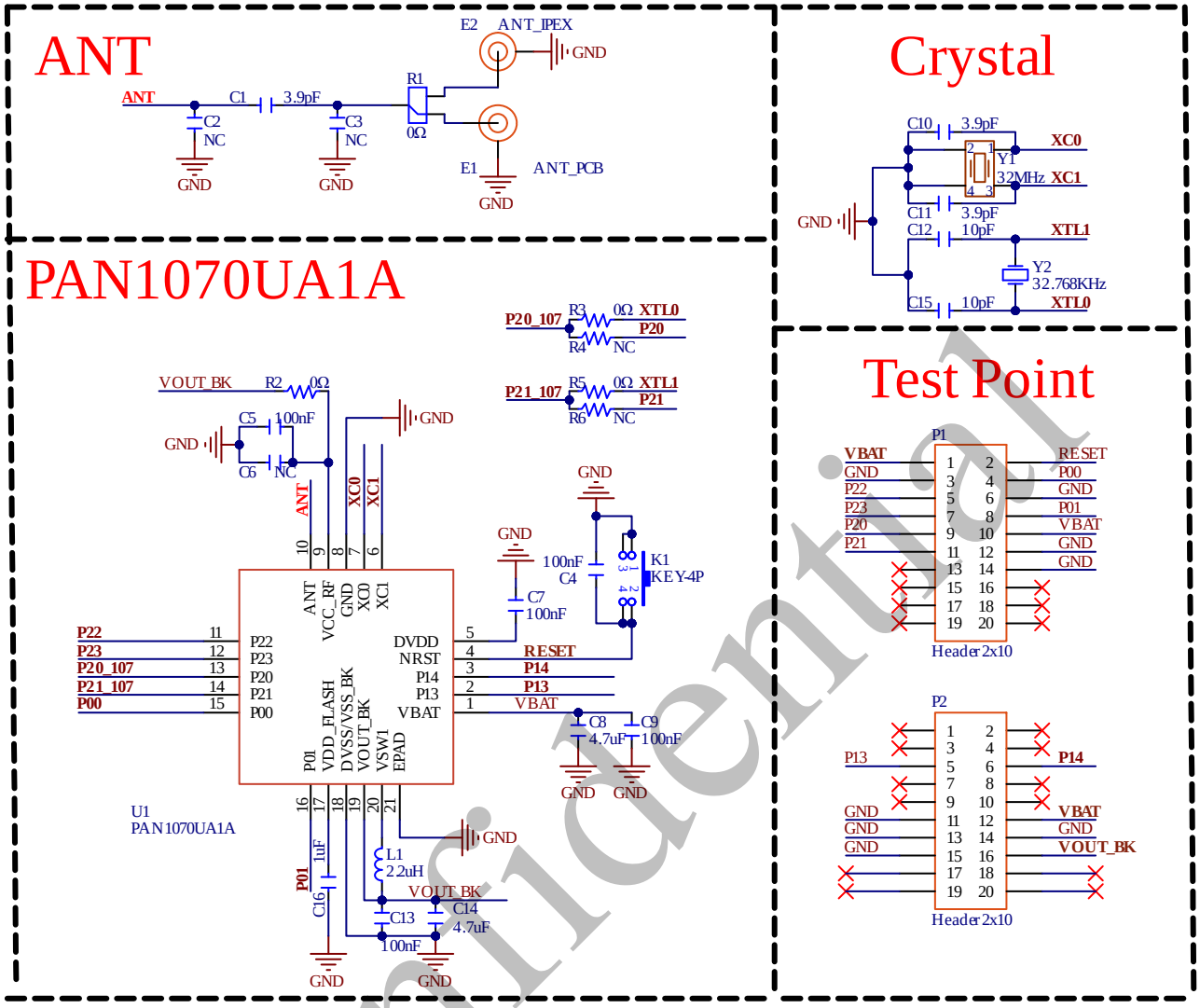


Figure 6-2 Application Schematic of the QFN20

7 Package Dimensions

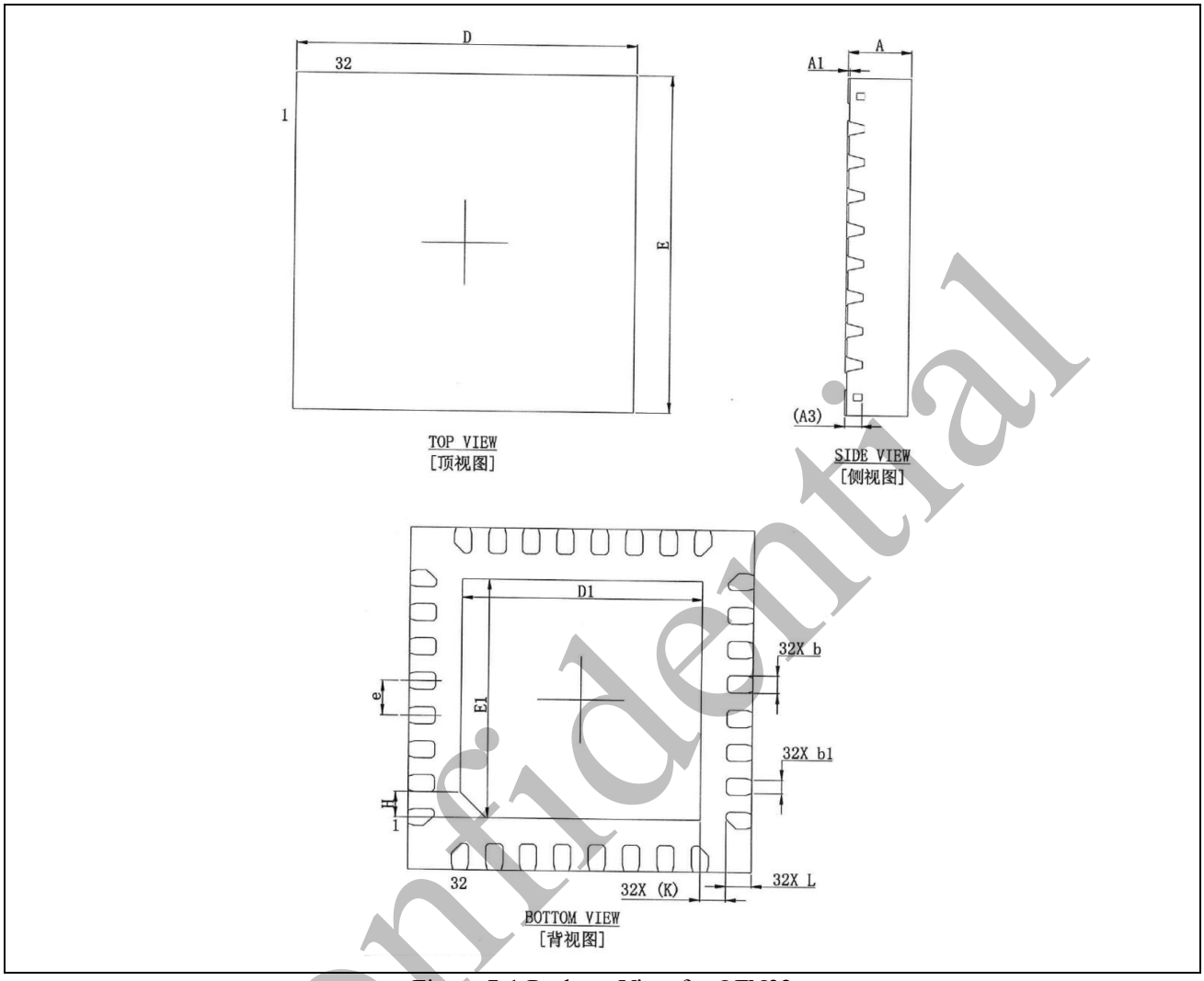


Figure 7-1 Package View for QFN32

Table 7-1 Package Dimension for QFN32

SYMBOL	MIN（mm）	NOM（mm）	MAX（mm）
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
b1	0.16 REF		
D	3.90	4.00	4.10
D1	2.70	2.80	2.90
E	3.90	4.00	4.10
E1	2.70	2.80	2.90
e	0.40 BSC		
K	0.30 REF		
L	0.20	0.30	0.40
H	0.30 REF		

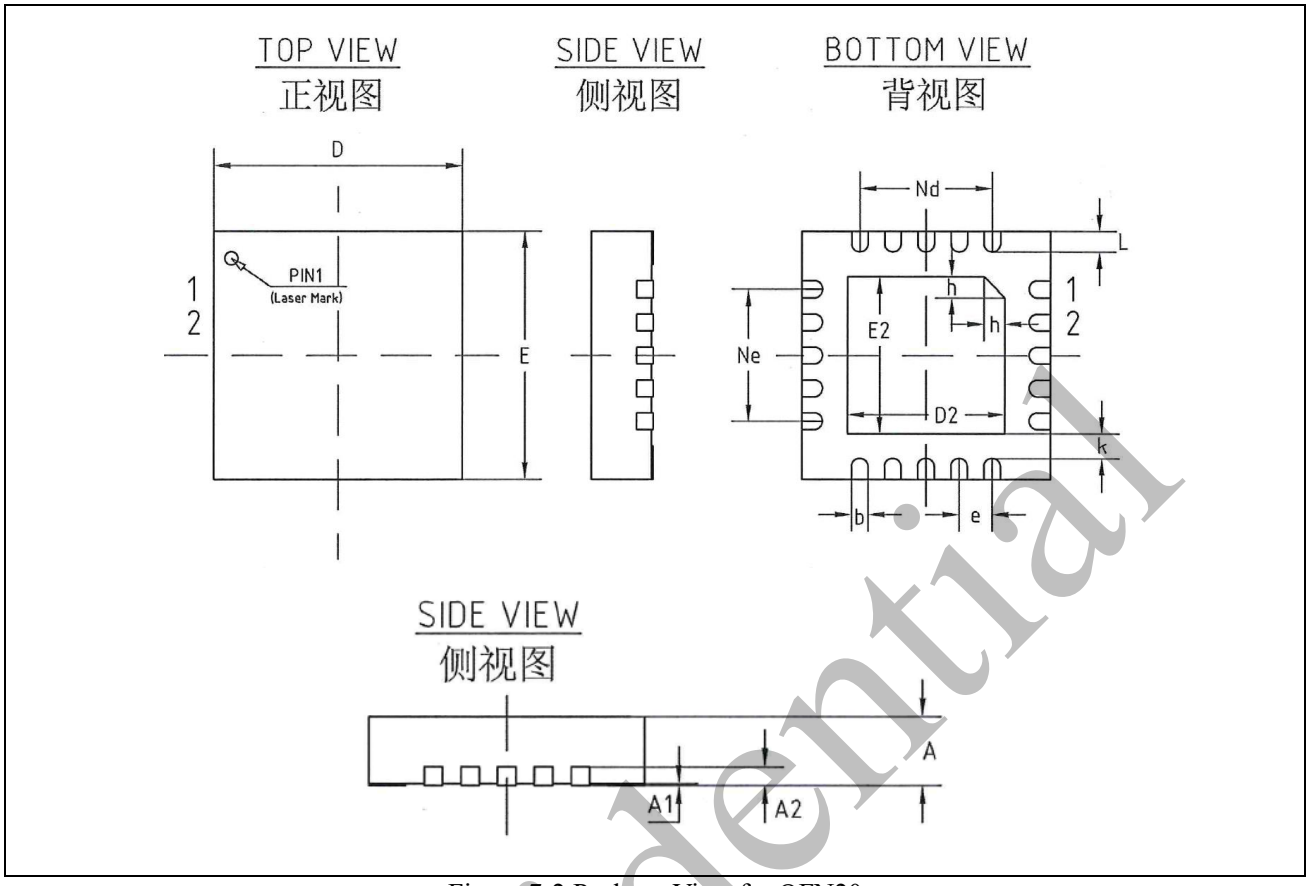


Figure 7-2 Package View for QFN20

Table 7-2 Package Dimension for QFN20

SYMBOL	MIN（mm）	NOM（mm）	MAX（mm）
A	0.70	0.75	0.80
A1	-	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
D2	1.80	1.90	2.00
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
e	0.40 BSC		
K	0.20	0.30	0.40
L	0.20	0.25	0.30
h	0.20	0.25	0.30
Ne	1.60 BSC		
Nd	1.60 BSC		

8 Precautions

1. This product is a CMOS device and should be protected against static electricity during storage, transportation and use.
2. Grounding when device is in use.
3. Reflow temperature can not exceed 260℃.

   The lead-free reflow soldering process is shown in the figure below:

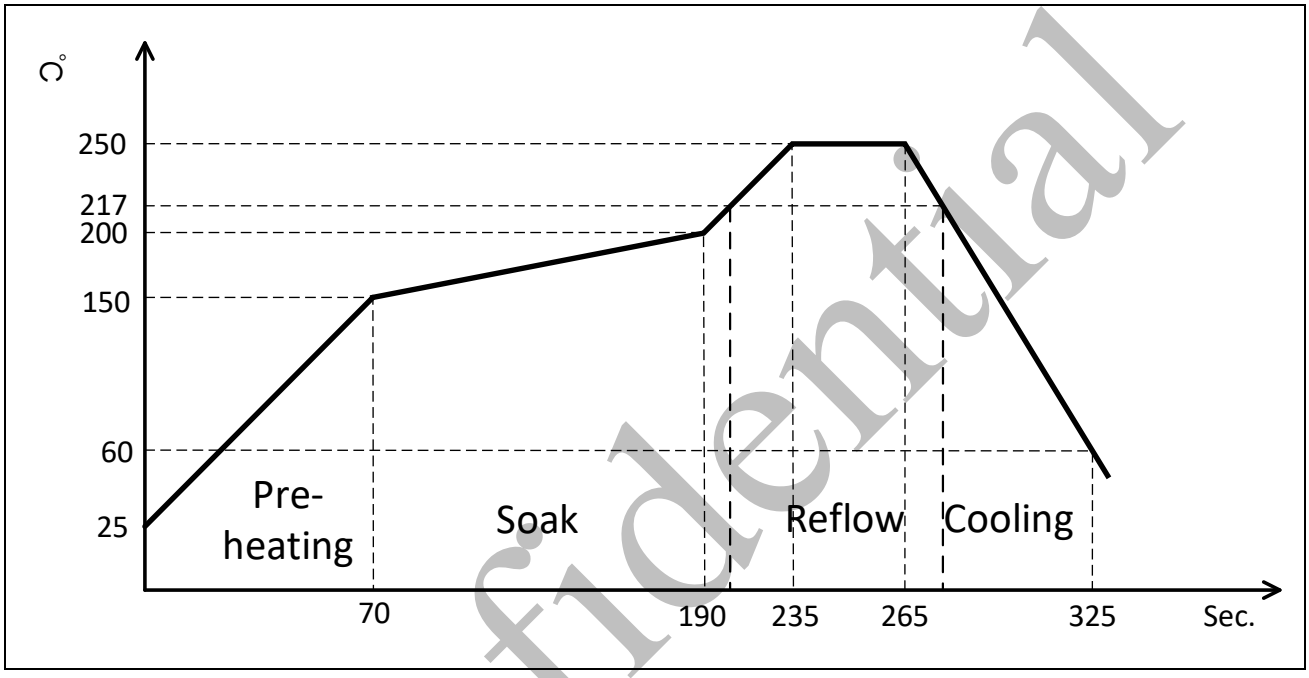


Figure 8-1 Reflow Profile

9 Storage Conditions

1. Products should be stored in sealed packages: when the temperature is less than 30 degrees and the humidity is less than 90%, it can last for 12 months.
2. After the package is opened, the components will be used in the reflow process or other high-temperature processes. The following conditions must be met:
   a. Completed within 72 hours and the factory environment is less than 30℃≤ 60% RH.
   b. Stored in 10% RH environment.
   c. Exhaust at 125℃ for 24 hours to remove internal water vapor before used.
3. MSL (Moisture Sensitivity Level): Level-3 (based on IPC/JEDEC J-STD-020)

Abbreviation

A	
APB	Advanced Peripheral Bus
ADC	Analog-to-Digital Converter
ALT	Alternate Function Select
ANAC	Analog Control
APROM	Application ROM
ATT	Attribute Protocol
B	
BAUDR	Baud Rate Select Register
BLDC	Brushless Direct Current Motor
Bluetooth LE	Bluetooth Low Energy
BOD	Brown-out Detector
BOM	Bill of Materials
C	
CFGx	Configuration Register for Channel x
ChEnReg	DMA Channel Enable Register
CMPDAT	Compare value
CPU	Central Processing Unit
CRC-32	Cyclic Redundancy Check
CTLx	Control Register for Channel x
CTRLR0	Control Register 0
CTRLR1	Control Register 1
D	
DARx	Destination Address Register for Channel x
Desiccant	A material for adsorbing moisture while remaining dry
DFBA	Data Flash Base Address Register
DLF	Divisor Latch Fraction Register
DLH	Divisor Latch High
DLL	Divisor Latch Low
DmaCfgReg	DMA Configuration Register
DMACR	DMA Control Register
DmaIdReg	DMA ID Register
DMARDLR	DMA Receive Data Level Register
DMASA	DMA Software Acknowledge
DMATDLR	DMA Transmit Data Level Register
DR	Data Register
DSTATARx	Destination Status Address Register for Channel x
DSTATx	Destination Status Register for Channel x
E	
ESD	Electro-Static discharge
F	
FCR	FIFO Control Register
FIFO	First Input First Output
FMC	Flash Memory Controller
Floor life	The longest time that the HiSilicon product is allowed to remain in the workshop (environ-ment <30 °C / 60% RH, before unpacking the moisture-proof packaging to reflow).
G	
GAP	Generic Access Profile
GATT	Generic Attribute Profile
GPIO	General-purpose I/O
H	
HCLK	Tstem Clock
HIC	Humidity Indicator Card
HID	Human Interface Device
HIRC	32MHz internal high speed osc-illator
HTX	Halt TX
HXT	32MHz external high speed crystal oscillator
I	
I2C	Inter-Integrated Circuit
IAP	In-Application-Programming
ICE	In-Circuit-Emulator
ICP	In-Circuit Programming
ICR	Interrupt Clear Register
IDR	Identification Register
IER	Interrupt Enable Register
IIR	Interrupt Identity Register
IMR	Interrupt Mask Register
IRSR	Interrupt Raw Status Registers
ISB	Instruction Synchronization Barrier
ISP	In-System Programming
ISR	Interrupt Service Routine
L	
L2CAP	Logical Link Control and Adaptation Protocol
LCR	Line Control Register
LCR_EXT	Line Extended Control Register
LDO	Low dropout regulator
LDROM	Loader ROM
LIRC	32 kHz internal low speed RC oscillator
LNA	Low Noise Amplifier

LSB	Least significant bit
LSR	Line Status Register
LstDstReg	Last Destination Transaction Request Register
LstSrcReg	Last Source Transaction Request Register
LVR	Low Voltage Reset
LXT	32.768 kHz external low speed crystal oscillator
M	
MBB	Moisture Barrier Bag
MCR	Modem Control Register
MCU	Micro Control Unit
MDM	Mobile Device Management
MFP	Multiple Function Port
MISO	Master input slave output
MOSI	Master output slave input
MSB	Most Significant Bit
MSL	Moisture sensitivity level, this product is on level 3
MSR	Modem Status Register
MSTICR	Multi-Master Interrupt Clear Register
N	
NMI	Non Maskable Interrupt
NVIC	Nested Vectored Interrupt Controller
P	
PA	Power Amplifier
PLL	Phase Locked Loop
POR	Power-on Reset
PWM	Pulse Width Modulation
R	
RAR	Receive Address Register
RBR	Receive Buffe Register
ReqDstReg	Destination Software Transaction Request Register
ReqSrcReg	Source Software Transaction Request Register
RF	Radio frequency
RFL	Receive FIFO Level
RISR	Raw Interrupt Status Register
ROM	Read-Only Memory
RSSI	Received Signal Strength Indication
RTOS	Real Time Operating System
RXFLR	Receive FIFO Level Register
RXFTLR	Receive FIFO Threshold Level Register
RXOICR	Receive FIFO Overflow Interrupt Clear Register
RXUICR	Receive FIFO Underflow Interrupt Clear Register
S	
SARx	Source Address Register for Channel x Register
SCB	System Control Block Registers
SCB	System Control Block Registers
SCR	Scratchpad Register
SER	Slave Enable Register
SglReqDstReg	Single Destination Transaction Request Register
SglReqSrcReg	Single Source Transaction Request Register
Shelf Life	Normal storage time after moisture-proof packaging
SM	Security Manager
SoC	System on chip
SPI	Serial Peripheral Interface
SPROM	Security protection ROM
SR	Status Register
SRAM	Static random access memory
SSTATARx	Source Status Address Register for Channel x
SSTATx	Source Status Register for Channel x
Statusint	Combined Interrupt Status Register
SWD	Serial Wire Debug
SysTick	System Timer
T	
TAR	Transmit Address Register
TFL	Transmit FIFO Level
THR	Transmit Holding Register
THRE	Transmitter Holding Register Empty
TMR	Timer Controller
TXFLR	Transmit FIFO Level Register
TXFTLR	Transmit FIFO Threshold Level Register
TXOICR	Transmit FIFO Overflow Interrupt Clear Register
U	
UART	Universal Asynchronous Receiver/Transmitters
USR	UART Status Register
W	
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Revision History

Version	Date	Content
1.0	Oct. 2023	Initial
1.1	Nov. 2023	Add the Application Reference Diagram. Corrected clerical error of pin12 and pin13 in the Pin Diagram. Corrected the name of pin31 in the Pin Diagram.
1.2	Dec. 2023	Update the Pin Information.
1.3	Jan. 2024	Add the PAN1070UAEC.
1.4	Mar. 2024	Add the Electrical specification.
1.5	Apr. 2024	Update the Key Features.
1.6	May. 2024	Update the Electrical specification. Update the Pin Diagram of the QFN20 package.

Internal version, for reference only.

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