



**PAN101x series**

# **Datasheet**

V1.6 Dec. 2024

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Panchip Microelectronics Co., Ltd.

**BLE SoC Transceiver**

## General Description

PAN101x series integrates BLE5.3 and 2.4GHz dual-mode wireless SoC transceiver. The transceiver works in the 2.400-2.483GHz universal ISM frequency band. There is a 256KB Flash program memory and a 16KB SRAM memory. In addition, PAN101x series is equipped with a wealth of peripherals, including up to 12 GPIOs, 8-channel PWM, one 32-bit timer, two 24-bit timers, one I2C, two UARTs, two SPIs, four external channels ADC, WDT, WWDT, USB2.0(Full Speed), 32K RC etc. PAN101x series is suitable for application of wireless mouse, smart home and electronic shelf label.

## Key Features

- **MCU**
  - 32-bit MCU core running up to 48MHz
- **Memory**
  - 256KB flash supporting deep power-down mode
  - 16KB SRAM
  - 128B eFuse
  - 4KB I-cache
- **Low Power**
  - Active mode RX: 2.5mA@1Mbps(DCDC)
  - Active mode TX at 0dBm: 5.06mA(DCDC)
  - Standby mode : 0.28uA
  - Standby mode(16K SRAM retention): 1.88uA (GPIO, XTL, RCL can wake up)
  - Deep sleep mode: 3.37uA (All Logic Retention, GPIO, XTL, RCL can wake up)
- **Clock**
  - 32MHz RC
  - 32MHz XTAL
  - 32kHz RC
  - 32.768kHz XTAL
  - DPLL(48MHz)
- **RF**
  - Mode
    - BLE5.3 modes: 1Mbps, 2Mbps, 500kbps, 125kbps
    - 2.4G private protocol: 1Mbps, 2Mbps 500kbps, 250kbps, 125kbps, supporting hardware ACK
  - Output power: up to 8.5dBm
  - Receiver
    - -98dBm@125kbps
    - -98dBm@500kbps
    - -95dBm@1Mbps
    - -92dBm@2Mbps
  - RSSI
    - Resolution: 0.25dB
    - Accuracy: ±2dB
    - Range: -90dbm ~ -15dBm
  - Single antenna supported
  - Safety regulations: BQB / ETSI / FCC
- **Peripheral**
  - Up to 12 GPIOs
  - 8-channel PWM
  - one 32-bit timer, two 24-bit timers
  - One I2C
  - Two UARTs
  - Two SPIs
  - 2-channel DMA
  - 9-channel ADC (4 ext, VBG\_1P2, VBG\_VT, 1/4VDD, VBG\_0P6, Temp2)
  - WDT / WWDT
  - IO / BOD / POR / LVR / System reset
  - FMC(Support IAP, support the boot loader with address 0x0)
  - Clock measurement and clock calibration
  - USB2.0(Full\_speed)
  - Flash data encryption
- **Temperature sensor**
  - Support temperature sensor
  - Test range: -40°C ~ 85°C
- **Power Management**
  - Integrated voltage regulator
  - Operating voltage: 1.8V to 3.6V (Support DCDC)
- **Package**
  - SSOP24 / MSOP10
- **Operating Condition**
  - Operating temperature: -40°C ~ 85°C
  - Storage temperature: -60°C~150°C

## Typical Applications

- Electronic Shelf Label
- Wireless mouse
- LED light control

## Bluetooth Features

### Bluetooth Low Energy Controller

The PAN101x series Bluetooth Low Energy Controller supports all low-energy features required by Bluetooth specification version 5.3. The controller supports the following:

- **Support 1M PHY, 2M PHY and Coded PHY (s2 and s8)**
- **Support Advertising, and Connection and Peripheral role**
- **Up to 2 Link Layer state machines concurrently:**
  - Advertising
  - Connection
- **Support LE Features:**
  - LL Encryption
  - LE Data Packet Length Extension
  - Channel Selection Algorithm #2
  - Constant Tone Extension
- **Support Update Channel Statistics**

### Bluetooth Host

- **Generic Access Profile (GAP) with all possible LE roles**
  - Peripheral
  - Broadcaster
- **GATT (Generic Attribute Profile)**

- Server (to be a sensor)
- Client (to connect to sensors)
- **Pairing support, including the Secure Connections feature from Bluetooth 4.2**
- **Non-volatile storage support for permanent storage of Bluetooth-specific settings and data**
- **Clean HCI driver abstraction**
  - 3-Wire (H5) & 5-Wire (H4) UART
  - SPI
  - Local controller support as a virtual HCI driver

## Proprietary Radio 2.4G Features

- Support 250K, 1M and 2M PHY
- XN297L, PAN1026 protocol compliant
- Support No Acknowledge, Acknowledge and Acknowledge with payload
- Support CRC8, CRC16 and CRC24
- Support whitening
- Compatible with Bluetooth frame structure, can simulate Bluetooth broadcast and scanning
- Compatible with Bluetooth Coded PHY S2/S8
- Supports 2-byte address
- Support the same spread spectrum function as the BLE protocol

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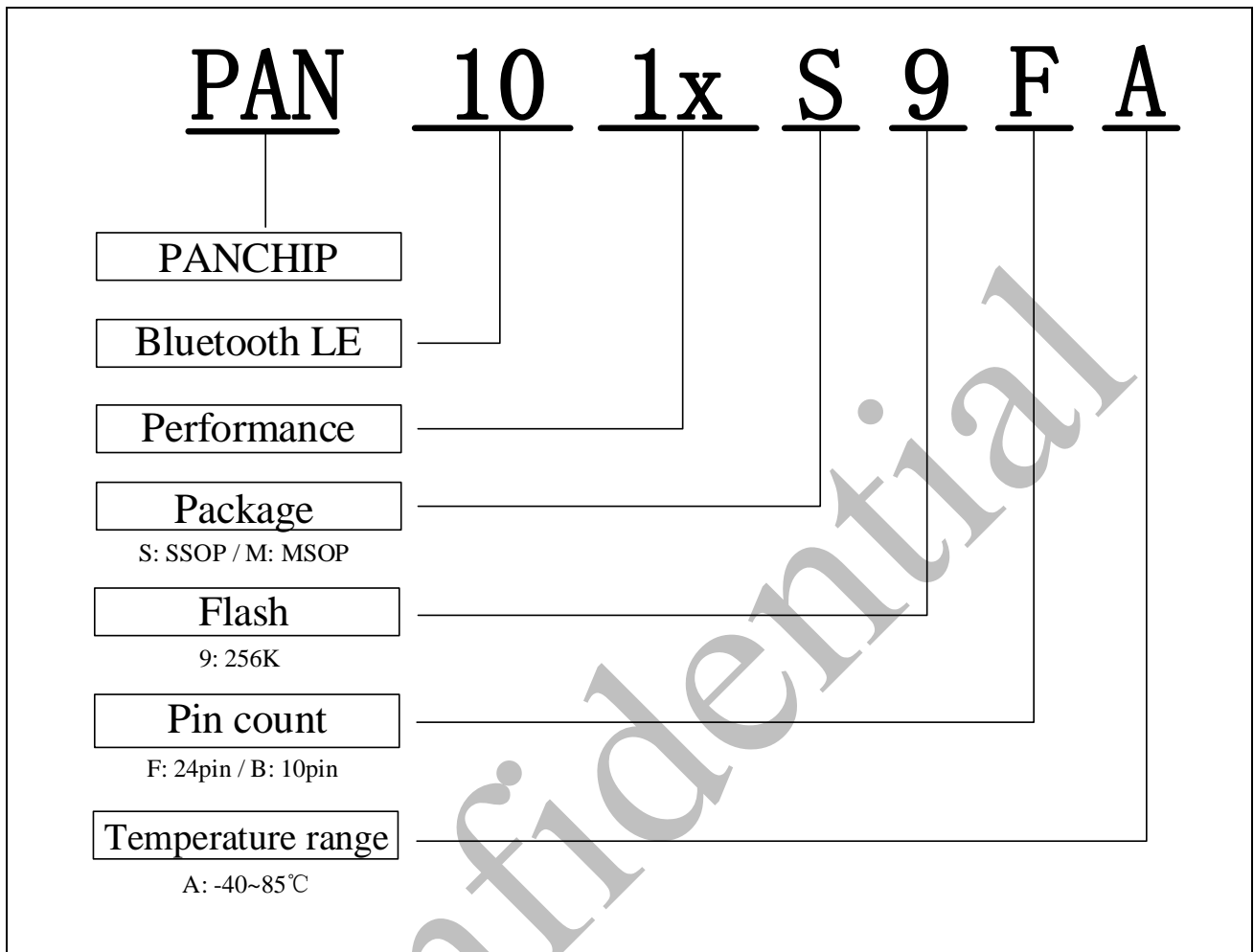
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## 1 Naming rule



## 2 Ordering information

Partnumber	Type	Pack- age	Pin Count	IO	FLASH	RAM	Temperature range	Packing
PAN1010S9FA	BLE5.3	SSOP	24	12	256K	16K	-40~85°C	TUBE
PAN1010M9BA	BLE5.3	MSOP	10	4	256K	16K	-40~85°C	Tape & Reel

*Before ordering, please contact the sales window for the latest mass production information.*

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### 3 Block Diagram

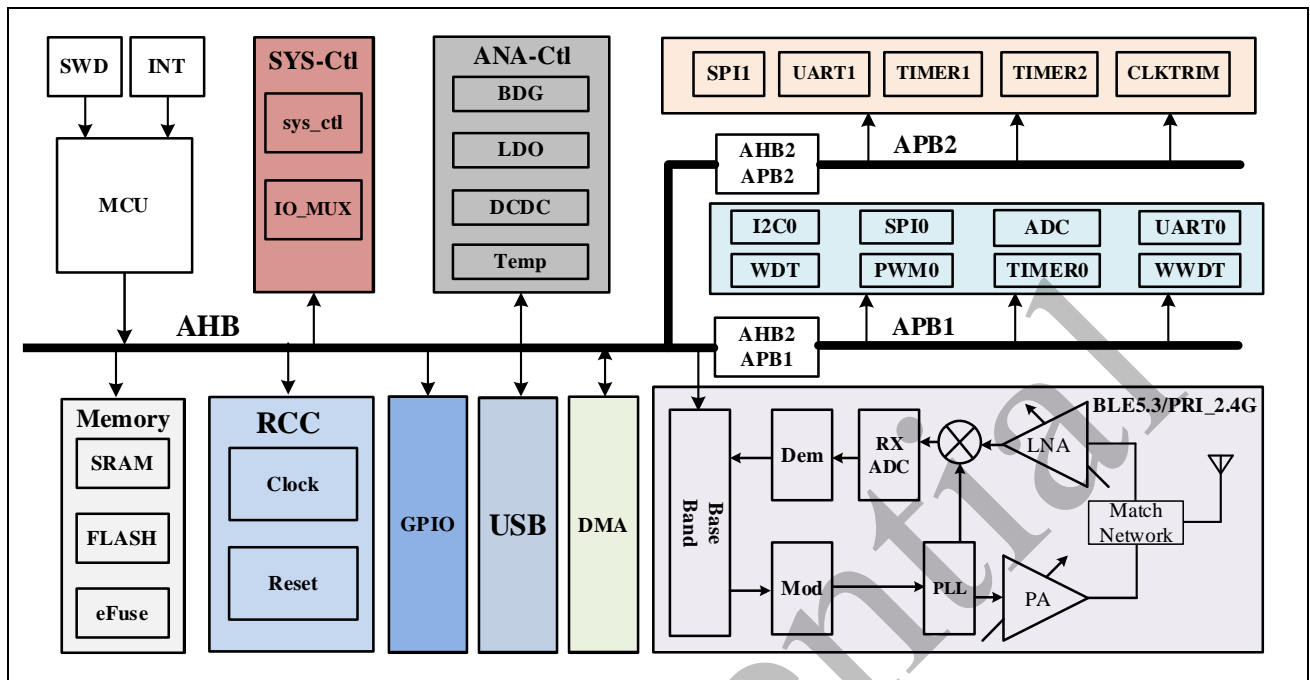


Figure 3-1 Block Diagram

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## 4 Pin Information

### 4.1 Pin Diagram

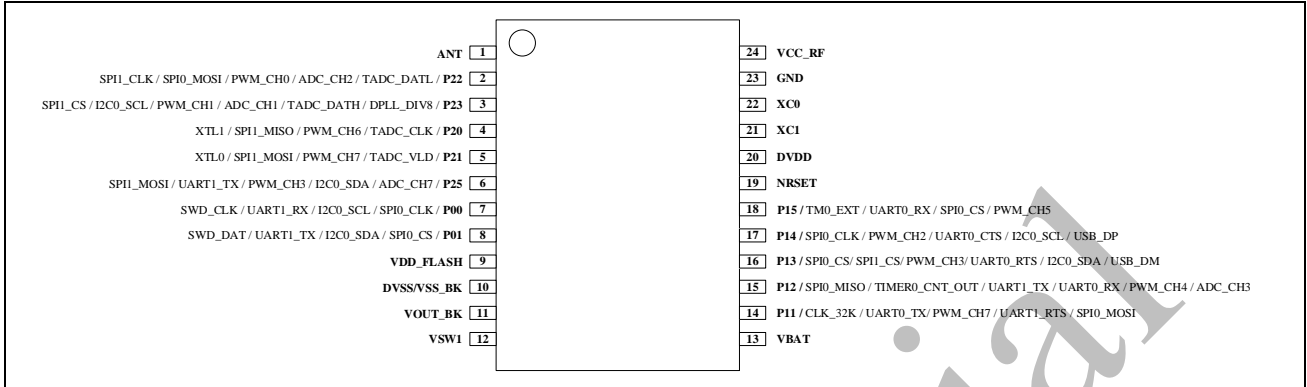


Figure 4-1 SSOP24 Diagram

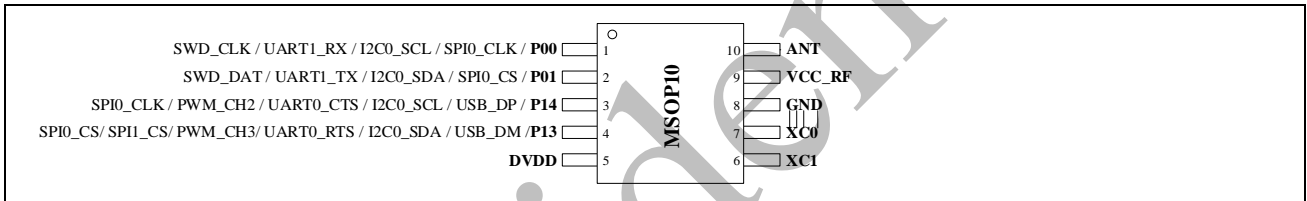


Figure 4-2 MSOP10 Diagram

## 4.2 Pin Descriptions

Detail pin descriptions see Table 4-1.

Table 4-1 Pin Descriptions

Pin No.		Pin Name	Pin Type	Description
SSOP24	MSOP10			
1	10	ANT	AI/AO	RF antenna , an external antenna is required for use
2	-	P22	I/O	General-purpose digital input and output
		SPI1_CLK	I/O	Spi1 clock
		PWM_CH0	O	Channel 0 PWM output
		SPI0_MOSI	I/O	Spi0 mosi
		ADC_CH2	AI	Channel 2 ADC input
3	-	P23	I/O	General-purpose digital input and output
		SPI1_CS	I/O	Spi1 cs
		PWM_CH1	O	Channel 1 PWM output
		DPLL_DIV8	O	Dpll_div8 output
		I2C0_SCL	I/O	I2c0 scl
		ADC_CH1	AI	Channel 1 ADC input
4	-	P20	I/O	General-purpose digital input and output
		XTL1	AO	External 32.768kHz clock source output
		SPI1_MISO	I/O	Spi1 miso
		PWM_CH6	O	Channel 6 PWM output
5	-	P21	I/O	General-purpose digital input and output
		XTL0	AI	External 32.768kHz clock source input
		SPI1_MOSI	I/O	Spi1 mosi
		PWM_CH7	O	Channel 7 PWM output
6	-	P25	I/O	General-purpose digital input and output
		UART1_TX	O	Uart1 tx
		SPI1_MOSI	I/O	Spi1 mosi
		PWM_CH3	O	Channel 3 PWM output
		I2C0_SDA	I/O	I2c0 sda
		ADC_CH7	AI	Channel 7 ADC input
7	1	P00	I/O	General-purpose digital input and output
		SWD_CLK	I	Swd clock input

		UART1_RX	I	Uart1 rx
		I2C0_SCL	I/O	I2c0 scl
		SPI0_CLK	I/O	Spi0 clock
8	2	P01	I/O	General-purpose digital input and output
		SWD_DAT	I/O	Swd data input and output
		UART1_TX	O	Uart1 tx
		I2C0_SDA	I/O	I2c0 sda
		SPI0_CS	I/O	Spi0 cs
9	-	VDD_FLASH	P	FLASH power input
10	-	DVSS/VSS_BK	P	Common ground terminal of DCDC power supply, independent power ground
11	-	VOUT_BK	P	DCDC voltage output
12	-	VSW1	P	DCDC internal power switch (switching frequency is about 650kHz), an external inductor is required when using
13	-	VBAT	P	Power input
14	-	P11	I/O	General-purpose digital input and output
		UART1_RTS	O	Uart1 rts
		SPI0_MOSI	I/O	Spi0 mosi
		PWM_CH7	O	Channel 7 PWM output
		CLK_32K	O	Clk_32k output
		UART0_TX	O	Uart0 tx
15	-	P12	I/O	General-purpose digital input and output
		UART0_RX	I	Uart0 rx
		TIMER0_CNT_OUT	O	Timer0 output
		UART1_TX	O	Uart1 tx
		SPI0_MISO	I/O	Spi0 miso
		PWM_CH4	O	Channel 4 PWM output
		ADC_CH3	AI	Channel 3 ADC input
16	4	P13	I/O	General-purpose digital input and output
		UART0_RTS	O	Uart0 rts
		I2C0_SDA	I/O	I2c0 sda
		PWM_CH3	O	Channel 3 PWM output
		SPI1_CS	I/O	Spi1 cs
		SPI0_CS	I/O	Spi0 cs

		USB_DM	AI/AO	Usb dm
17	3	P14	I/O	General-purpose digital input and output
		UART0_CTS	I	Uart0 cts
		I2C0_SCL	I/O	I2c0 scl
		PWM_CH2	O	Channel 2 PWM output
		SPI0_CLK	I/O	Spi0 clock
		USB_DP	AI/AO	Usb dp
18	-	P15	I/O	General-purpose digital input and output
		SPI0_CS	I/O	Spi0 cs
		PWM_CH5	O	Channel 5 PWM output
		TM0_EXT	I	Timer0 external input
		UART0_RX	I	Uart0 rx
19	-	NRSET	I	Reset pin
20	5	DVDD	P	Hldo output , typical value 1.2V
21	6	XC1	AO	External 32MHz clock source output
22	7	XC0	AI	External 32MHz clock source input
23	8	GND	P	Ground
24	9	VCC_RF	P	RF power input, can be directly connected to VOUT_BK

## 5 Electrical specification

### Maximum and minimum values

In the notes below each table, the data obtained through comprehensive evaluation, design simulation and/or process features are not tested on the production line; based on the comprehensive evaluation, the minimum and maximum values are after the sample test. Take the average value and add and subtract three times the standard distribution (average  $\pm 3 \Sigma$ ).

### 5.1 RF characteristics

Table 5-1 RF characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$f_{OP}$	Operating frequency		2400	-	2483	MHz
PLLres	PLL programming resolution		244	1M	-	Hz
DR	Data rate		0.125	-	2	Mbps
$\Delta f_{BLE,2M}$	Frequency deviation @ BLE 2Mbps		450	500	550	kHz
$\Delta f_{BLE,1M}$	Frequency deviation @ BLE 1Mbps		225	250	275	kHz
$\Delta f_{297,2M}$	Frequency deviation @ 297mode 2Mbps		450	500	550	kHz
$\Delta f_{297,1M}$	Frequency deviation @ 297mode 1Mbps		225	250	275	kHz
$\Delta f_{N,2M}$	Frequency deviation @ N-mode 2Mbps		-	320	-	kHz
$\Delta f_{N,1M}$	Frequency deviation @ N-mode 1Mbps		-	170	-	kHz
$\Delta f_{BLE,2M}$	Channel spacing @ BLE 2Mbps		-	2	-	MHz
$\Delta f_{BLE,1M}$	Channel spacing @ BLE 1Mbps		-	2	-	MHz
$\Delta f_{297,2M}$	Channel spacing @ 297mode 2Mbps		-	2	-	MHz
$\Delta f_{297,1M}$	Channel spacing @ 297mode 1Mbps		-	1	-	MHz
$\Delta f_{N,2M}$	Channel spacing @ N-mode 2Mbps		-	2	-	MHz
$\Delta f_{N,1M}$	Channel spacing @ N-mode 1Mbps		-	1	-	MHz

Table 5-2 TX characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$P_{RFTX}$	Output power		-	-	8.5	dBm
$P_{RFC}$	RF power control range		-	40	-	dB
$P_{RFCR}$	RF power accuracy		-	-	$\pm 3$	dB
$P_{RF1M,1}$	1st Adjacent Channel Transmit Power @1Mbps		-	-40	-	dBc
$P_{RF1M,2}$	2nd Adjacent Channel Transmit Power @1Mbps		-	-56	-	dBc
$P_{RF1M,\geq 3}$	3rd Adjacent Channel Transmit Power @1Mbps		-	-60	-	dBc

P <sub>RF2M,2</sub>	1st Adjacent Channel Transmit Power @2Mbps	-	-37	-	dBc
P <sub>RF2M,4</sub>	2nd Adjacent Channel Transmit Power @2Mbps	-	-58	-	dBc
P <sub>RF2M,≥6M</sub>	3rd Adjacent Channel Transmit Power @2Mbps	-	-60	-	dBc
P <sub>BW1M</sub>	20dB bandwidth @1Mbps	-	1.3	-	MHz
P <sub>BW2M</sub>	20dB bandwidth @2Mbps	-	2.3	-	MHz
P <sub>SP,1</sub>	Spurious @≤1GHz	-	-	-73	dBm
P <sub>SP,2</sub>	Spurious @≥1GHz	-	-	-49	dBm

Table 5-3 RX characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
P <sub>RX,MIX</sub>	Receive maximum input power		-	0	-	dBm
P <sub>SENS,1M,BLE</sub>	Sensitivity, 1Mbps BLE		-	-95	-	dBm
P <sub>SENS,2M,BLE</sub>	Sensitivity, 2Mbps BLE		-	-92	-	dBm
P <sub>SENS,125K,BLE</sub>	Sensitivity, 125kbps BLE		-	-98	-	dBm
P <sub>SENS,500K,BLE</sub>	Sensitivity, 500kbps BLE		-	-98	-	dBm
P <sub>SENS,250K,B</sub>	Sensitivity, 250kbps B mode		-	-98	-	dBm
P <sub>SENS,1M,297</sub>	Sensitivity, 1Mbps 297 mode	Sensitivity, 1Mbps ideal transmitter, ≤37 bytes, BER = 0.1% is presented.	-	-92	-	dBm
P <sub>SENS,2M,297</sub>	Sensitivity, 2Mbps 297 mode		-	-90	-	dBm
P <sub>SENS,250K,297</sub>	Sensitivity, 250kbps 297 mode		-	-98	-	dBm
P <sub>SENS,1M,N</sub>	Sensitivity, 1Mbps N-mode		-	-92	-	dBm
P <sub>SENS,2M,N</sub>	Sensitivity, 2Mbps N-mode		-	-90	-	dBm
P <sub>SENS,250K,N</sub>	Sensitivity, 250kbps N-mode		-	-98	-	dBm
C/I <sub>CO,1M,BLE</sub>	Co-Channel interference@1Mbps		-	6	-	dB
C/I <sub>1M,1M,BLE</sub>	Adjacent (1 MHz) interference@1Mbps		-	-3	-	dB
C/I <sub>2M,1M,BLE</sub>	Adjacent (2 MHz) interference @1Mbps		-	-40	-	dB
C/I <sub>≥3M,1M,BLE</sub>	Adjacent (≥3 MHz) interference @1Mbps		-	-45	-	dB
C/I <sub>Image,1M,BLE</sub>	Image frequency interference @1Mbps		-	-23	-	dB
C/I <sub>Image±1M,1M,BLE</sub>	Adjacent (±1MHz) interference to in-band image frequency @1Mbps		-	-38	-	dB
C/I <sub>≥6M,1M,BLE</sub>	Adjacent (≥6 MHz) interference @1Mbps		-	-45	-	dB
C/I <sub>CO,2M,BLE</sub>	Co-Channel interference @2Mbps		-	7	-	dB
C/I <sub>2M,2M,BLE</sub>	Adjacent (2 MHz) interference @2Mbps		-	-3	-	dB
C/I <sub>4M,2M,BLE</sub>	Adjacent (4 MHz) interference @2Mbps		-	-37	-	dB

$C/I_{\geq 6M,2M,BLE}$	Adjacent ( $\geq 6$ MHz) interference @2Mbps	-	-35	-	dB
$C/I_{Image,2M,BLE}$	Image frequency interference @2Mbps	-	-23	-	dB
$C/I_{Image\pm 2M,2M,BLE}$	Adjacent ( $\pm 2$ MHz) interference to in-band image frequency	-	-36	-	dB
$C/I_{\geq 12M,2M,BLE}$	Adjacent ( $\geq 12$ MHz) interference @2Mbps	-	-35	-	dB
$C/I_{CO,125K,BLE}$	Co-Channel interference @125kbps	-	-6	-	dB
$C/I_{1M,125K,BLE}$	Adjacent (1 MHz) interference @125kbps	-	-13	-	dB
$C/I_{2M,125K,BLE}$	Adjacent (2 MHz) interference @125kbps	-	-37	-	dB
$C/I_{\geq 3M,125K,BLE}$	Adjacent ( $\geq 3$ MHz) interference @125kbps	-	-49	-	dB
$C/I_{Image,125K,BLE}$	Image frequency interference @125kbps	-	-31	-	dB
$C/I_{Image\pm 1M,125K,BLE}$	Adjacent ( $\pm 1$ MHz) interference to in-band image frequency @125kbps	-	-48	-	dB
$C/I_{CO,500K,BLE}$	Co-Channel interference @500kbps	-	1	-	dB
$C/I_{1M,500K,BLE}$	Adjacent (1 MHz) interference @500kbps	-	-6	-	dB
$C/I_{2M,500K,BLE}$	Adjacent (2 MHz) interference @500kbps	-	-31	-	dB
$C/I_{\geq 3M,500K,BLE}$	Adjacent ( $\geq 3$ MHz) interference @500kbps	-	-43	-	dB
$C/I_{Image,500K,BLE}$	Image frequency interference @500kbps	-	-25	-	dB
$C/I_{Image\pm 1M,500K,BLE}$	Adjacent ( $\pm 1$ MHz) interference to in-band image frequency @500kbps	-	-41	-	dB
$C/I_{CO,1M,297}$	Co-Channel interference @1Mbps	-	TBD	-	dB
$C/I_{1M,1M,297}$	Adjacent (1 MHz) interference @1Mbps	-	TBD	-	dB
$C/I_{2M,1M,297}$	Adjacent (2 MHz) interference @1Mbps	-	TBD	-	dB
$C/I_{\geq 3M,1M,297}$	Adjacent ( $\geq 3$ MHz) interference @1Mbps	-	TBD	-	dB
$C/I_{Image,1M,297}$	Image frequency interference @1Mbps	-	TBD	-	dB
$C/I_{Image\pm 1M,1M,297}$	Adjacent ( $\pm 1$ MHz) interference to in-band image frequency @1Mbps	-	TBD	-	dB
$C/I_{\geq 6M,1M,297}$	Adjacent ( $\geq 6$ MHz) interference @1Mbps	-	TBD	-	dB
$C/I_{CO,2M,297}$	Co-Channel interference @2Mbps	-	TBD	-	dB
$C/I_{2M,2M,297}$	Adjacent (2 MHz) interference @2Mbps	-	TBD	-	dB
$C/I_{4M,2M,297}$	Adjacent (4 MHz) interference @2Mbps	-	TBD	-	dB
$C/I_{\geq 6M,2M,297}$	Adjacent ( $\geq 6$ MHz) interference @2Mbps	-	TBD	-	dB
$C/I_{Image,2M,297}$	Image frequency interference @2Mbps	-	TBD	-	dB
$C/I_{Image\pm 2M,2M,297}$	Adjacent ( $\pm 2$ MHz) interference to in-band image frequency @2Mbps	-	TBD	-	dB
$C/I_{\geq 12M,2M,297}$	Adjacent ( $\geq 12$ MHz) interference @2Mbps	-	TBD	-	dB
$C/I_{CO,250K,297}$	Co-Channel interference @250kbps	-	TBD	-	dB



$C/I_{1M,250K,297}$	Adjacent (1 MHz) interference @250kbps	-	TBD	-	dB
$C/I_{2M,250K,297}$	Adjacent (2 MHz) interference @250kbps	-	TBD	-	dB
$C/I_{\geq 3M,250K,297}$	Adjacent ( $\geq 3$ MHz) interference @250kbps	-	TBD	-	dB
$C/I_{Image,250K,297}$	Image frequency interference @250kbps	-	TBD	-	dB
$C/I_{Image\pm 1M,250K,297}$	Adjacent ( $\pm 1$ MHz) interference to in-band image frequency @250kbps	-	TBD	-	dB
$C/I_{CO,1M,N}$	Co-Channel interference @1Mbps	-	TBD	-	dB
$C/I_{1M,1M,N}$	Adjacent (1 MHz) interference @1Mbps	-	TBD	-	dB
$C/I_{2M,1M,N}$	Adjacent (2 MHz) interference @1Mbps	-	TBD	-	dB
$C/I_{\geq 3M,1M,N}$	Adjacent ( $\geq 3$ MHz) interference @1Mbps	-	TBD	-	dB
$C/I_{Image,1M,N}$	Image frequency interference @1Mbps	-	TBD	-	dB
$C/I_{Image\pm 1M,1M,N}$	Adjacent ( $\pm 1$ MHz) interference to in-band image frequency @1Mbps	-	TBD	-	dB
$C/I_{\geq 6M,1M,N}$	Adjacent ( $\geq 6$ MHz) interference @1Mbps	-	TBD	-	dB
$C/I_{CO,2M,N}$	Co-Channel interference @2Mbps	-	TBD	-	dB
$C/I_{2M,2M,N}$	Adjacent (2 MHz) interference @2Mbps	-	TBD	-	dB
$C/I_{4M,2M,N}$	Adjacent (4 MHz) interference @2Mbps	-	TBD	-	dB
$C/I_{\geq 6M,2M,N}$	Adjacent ( $\geq 6$ MHz) interference @2Mbps	-	TBD	-	dB
$C/I_{Image,2M,N}$	Image frequency interference @2Mbps	-	TBD	-	dB
$C/I_{Image\pm 2M,2M,N}$	Adjacent ( $\pm 2$ MHz) interference to in-band image frequency @2Mbps	-	TBD	-	dB
$C/I_{\geq 12M,2M,N}$	Adjacent ( $\geq 12$ MHz) interference @2Mbps	-	TBD	-	dB
$C/I_{CO,250K,N}$	Co-Channel interference @250kbps	-	TBD	-	dB
$C/I_{1M,250K,N}$	Adjacent (1 MHz) interference @250kbps	-	TBD	-	dB
$C/I_{2M,250K,N}$	Adjacent (2 MHz) interference @250kbps	-	TBD	-	dB
$C/I_{\geq 3M,250K,N}$	Adjacent ( $\geq 3$ MHz) interference @250kbps	-	TBD	-	dB
$C/I_{Image,250K,N}$	Image frequency interference @250kbps	-	TBD	-	dB
$C/I_{Image\pm 1M,250K,N}$	Adjacent ( $\pm 1$ MHz) interference to in-band image frequency @250kbps	-	TBD	-	dB
$C/I_{CO,250K,B}$	Co-Channel interference @250kbps	-	TBD	-	dB
$C/I_{1M,250K,B}$	Adjacent (1MHz) interference @250kbps	-	TBD	-	dB
$C/I_{2M,250K,B}$	Adjacent (2MHz) interference @250kbps	-	TBD	-	dB
$C/I_{\geq 3M,250K,B}$	Adjacent ( $\geq 3$ MHz) interference @250kbps	-	TBD	-	dB
$C/I_{Image,250K,B}$	Image frequency interference @250kbps	-	TBD	-	dB
$C/I_{Image\pm 1M,250K,B}$	Adjacent ( $\pm 1$ MHz) interference to in-band image frequency @250kbps	-	TBD	-	dB

P <sub>IMD,5TH,1M</sub>	IMD performance 5 MHz offset @1Mbps	-	TBD	-	dBm
P <sub>IMD,5TH,2M</sub>	IMD performance 10 MHz offset @2Mbps	-	TBD	-	dBm

Table 5-4 RSSI characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
RSSI <sub>RF</sub>	RSSI indication range		-90	-	-15	dBm
RSSI <sub>Auu</sub>	RSSI accuracy		-	±2	-	dB
RSSI <sub>Res</sub>	RSSI resolution		-	0.25	-	dB
RSSI <sub>per</sub>	RSSI Sample period		-	0.25	-	us

Table 5-5 RF Timing characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
T <sub>OSC,EN</sub>	Crystal oscillator settling time		-	TBD	-	us
T <sub>TX,EN</sub>	Time between TXEN task and READY event after channel FREQUENCY configured		-	TBD	-	us
T <sub>RX,EN</sub>	Time between the RXEN task and READY event after channel FREQUENCY configured in default mode		-	TBD	-	us
T <sub>TX,DISABLE</sub>	Time between DISABLE task and DISABLED event when the radio was in TX		-	TBD	-	us
T <sub>RX,DISABLE</sub>	Time between DISABLE task and DISABLED event when the radio was in RX		-	TBD	-	us
T <sub>RX-TX</sub>	The time taken to switch from RX to TX or TX to RX		-	150	-	us

Table 5-6 RF power characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
I <sub>TX,P9dBm,DCDC</sub>	TX only run current 9dBm @DC-DC		-	13.97	-	mA
I <sub>TX,P6dBm,DCDC</sub>	TX only run current 6dBm @DC-DC		-	9.59	-	mA
I <sub>TX,P4dBm,DCDC</sub>	TX only run current 4dBm @DC-DC		-	6.67	-	mA
I <sub>TX,P0dBm,DCDC</sub>	TX only run current 0dBm @DC-DC		-	5.06	-	mA
I <sub>TX,P-4dBm,DCDC</sub>	TX only run current -4dBm @DC-DC		-	2.56	-	mA
I <sub>TX,P-8dBm,DCDC</sub>	TX only run current -8dBm @DC-DC		-	2.15	-	mA
I <sub>TX,P-12dBm,DCDC</sub>	TX only run current -12dBm @DC-DC		-	1.87	-	mA
I <sub>TX,P-16dBm,DCDC</sub>	TX only run current -16dBm @DC-DC		-	1.64	-	mA
I <sub>TX,P-20dBm,DCDC</sub>	TX only run current -20dBm @DC-DC		-	1.53	-	mA

$I_{TX,P-40dBm,DCDC}$	TX only run current -40dBm @DC-DC	-	1.12	-	mA
$I_{TX,P9dBm,LDO}$	TX only run current 9dBm @LDO	-	35.55	-	mA
$I_{TX,P6dBm,LDO}$	TX only run current 6dBm @LDO	-	16.28	-	mA
$I_{TX,P4dBm,LDO}$	TX only run current 4dBm @LDO	-	12.1	-	mA
$I_{TX,P0dBm,LDO}$	TX only run current 0dBm @LDO	-	9.43	-	mA
$I_{TX,P-4dBm,LDO}$	TX only run current -4dBm @LDO	-	5.74	-	mA
$I_{TX,P-8dBm,LDO}$	TX only run current -8dBm @LDO	-	5.08	-	mA
$I_{TX,P-12dBm,LDO}$	TX only run current -12dBm @LDO	-	4.62	-	mA
$I_{TX,P-16dBm,LDO}$	TX only run current -16dBm @LDO	-	4.04	-	mA
$I_{TX,P-20dBm,LDO}$	TX only run current -20dBm @LDO	-	3.92	-	mA
$I_{TX,P-40dBm,LDO}$	TX only run current -40dBm @LDO	-	3.00	-	mA
$I_{RX,1M,DCDC}$	RX 1Mbps current @DC-DC	-	2.50	-	mA
$I_{RX,2M,DCDC}$	RX 2Mbps current @DC-DC	-	2.71	-	mA
$I_{RX,1M,LDO}$	RX 1Mbps current @LDO	-	4.82	-	mA
$I_{RX,2M,LDO}$	RX 2Mbps current @LDO	-	5.67	-	mA
<p>Test conditions and methods.</p> <ol style="list-style-type: none"> <li>1. Transceiver power consumption tested in 1M mode using BLE ADV broadcast mode.</li> <li>2. 2M mode is used is the power consumption when BLE connection.</li> <li>3. The power consumption tested is the RF peak power.</li> <li>4. The test method uses the total power consumption minus the power consumption of the MCU when the RF is not operating to calculate the final power consumption.</li> <li>5. The sample software tested is based on peripheral_hr.</li> <li>6. 3.3V Power Supply</li> </ol>					

## 5.2 GPIO characteristics

Table 5-7 GPIO characteristics (single IO)

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$V_{IH}$	Input high voltage	$T_A=25^{\circ}C$	$0.7*VDD$	-	VDD	V
$V_{IL}$	Input low voltage	Load capacitance =20pF, $T_A=25^{\circ}C$	VSS	-	$0.2*VDD$	V
$V_{HYS}$	Input hysteresis voltage, $V_{hys}=V_{IH}-V_{IL}$	$T_A=25^{\circ}C$	-	-	$0.3*VDD$	V
$C_{Iana}$	Analog input capacitors	$T_A=25^{\circ}$	-	300	-	fF
$I_{Lkg}$	Leakage current, open-drain mode or input mode	$VDD \leq V_{IN} \leq 3.6V$	-	-	TBD	uA
$R_{PU}$	Pull-up resistor	$V_{in} = VSS,$ $VDD = 3.3V$	-	50	-	k $\Omega$
$R_{PD}$	Pull-down resistor	$V_{in} = VSS,$ $VDD = 3.3V$	-	100	-	k $\Omega$

$V_I$	Input voltage	$T_A=25^\circ\text{C}$	VSS	-	VDD	V
$V_O$	Output voltage	$T_A=25^\circ\text{C}$	VSS	-	VDD	V
$I_{\text{source}}$	Source current (Push-pull output) (Except for P03, P15)	$V_{in} = VDD-0.5V$	8.5	9.5	10.5	mA
$I_{\text{source}}$	Source current (Push-pull output) (P03, P15)	$V_{in} = VDD-0.5V$	21	22	23	mA
$I_{\text{sink}}$	Sink current (Push-pull output)	$V_{in} = VSS+0.5V,$ $T_A=25^\circ\text{C}$	19.5	20.5	21.5	mA
$f_{\text{Port\_CLK}}$	IO output frequency	Load capacitance $=20\text{pF}$	-	-	48	MHz

**Table 5-8 Combined test**

Description	Conditions	Status	Remark
IO default state after power on	$VDD=3.3V, T_A=25^\circ\text{C}$	P00, P01: Pull-up input state Others: High resistance state	
IO status in deepsleep mode	$VDD=3.3V, T_A=25^\circ\text{C}$	Deepsleep: All gpio retention Standby_m1: All gpio retention Standby_m0: P00, P01, P02 retention	
IO status at reset	$VDD=3.3V, T_A=25^\circ\text{C}$	P00, P01: Pull-up input state Others: High resistance state	

**Table 5-9 nRESET Input Characteristics**

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$V_{ILR}$	Negative threshold voltage, nRESET	$VDD=1.8V-3.3V, T_A=25^\circ\text{C}$	-	-	$0.22*VDD$	V
$V_{IHR}$	Positive threshold voltage, nRESET	$VDD=1.8V-3.3V, T_A=25^\circ\text{C}$	$0.48*VDD$	-	-	V
$V_{\text{hys\_rst}}$	Schmitt Trigger Voltage Hysteresis	$VDD=1.8V-3.3V, T_A=25^\circ\text{C}$	-	-	$0.26*VDD$	V
$R_{RST}$	nRESET pin internal pull-up resistor	$VDD=3.3V, T_A=25^\circ\text{C}$	-	7.5	-	$k\Omega$
$t_{FR, 0.3pF}$	nRESET pin input filter pulse time	$VDD=3.3V, T_A=25^\circ\text{C}$	-	TBD	-	ns

### 5.3 Reset characteristics

Table 5-10 Reset characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V <sub>BOD</sub>	Brown-out detection voltage threshold	BODSEL<2:0> = 000(falling edge), dVDD/dt≤3V/s	-	1.84	-	V
		BODSEL<2:0> = 001(falling edge), dVDD/dt≤3V/s	-	1.962	-	
		BODSEL<2:0> = 010(falling edge), dVDD/dt≤3V/s	-	2.053	-	
		BODSEL<2:0> = 011(falling edge), dVDD/dt≤3V/s	-	2.16	-	
		BODSEL<2:0> = 100(falling edge), dVDD/dt≤3V/s	-	2.252	-	
		BODSEL<2:0> = 101(falling edge), dVDD/dt≤3V/s	-	2.354	-	
		BODSEL<2:0> = 110(falling edge), dVDD/dt≤3V/s	-	2.466	-	
V <sub>BODhys</sub>	BOD hysteresis voltage	dVDD/dt≤3V/s	100	-	160	mV
T <sub>BOD_REI</sub>	BOD response Time(Normal mode)	dVDD/dt≤3V/s	1	32	32	Slow clock
I <sub>BOD</sub>	BOD operating current	dVDD/dt≤3V/s	-	0.5	-	uA
V <sub>POR</sub>	Power on reset voltage threshold	rising edge, dVDD/dt≤3V/s	-	1.71	-	V
		falling edge, dVDD/dt≤3V/s	-	1.69	-	V
T <sub>POR</sub>	POR settling time	V <sub>BAT</sub> = 3.3V	-	1.12	-	ms
V <sub>LVR</sub>	LVR detection voltage threshold	falling edge, dVDD/dt≤3V/s	-	1.85	-	V
T <sub>LVR_RE</sub>	LVR response time	T <sub>A</sub> = 25°C, dVDD/dt≤3V/s	1	32	32	Slow clock
I <sub>LVR</sub>	LVR operating current	T <sub>A</sub> = 25°C, dVDD/dt≤3V/s	-	0.1	-	uA

### 5.4 Clock characteristics

Table 5-11 HXTAL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f <sub>HXTL</sub>	High speed crystal oscillator (HXTAL) frequency	VDD=3.3V, T <sub>A</sub> =25°C	-	32	-	MHz
C <sub>LoadHXTL</sub>	Crystal load capacitance	VDD=3.3V, T <sub>A</sub> =25°C	7	9	12	pF
I <sub>DDHXTL</sub>	HXTAL oscillator operating current	VDD=3.3V, T <sub>A</sub> =25°C	-	250	-	μA
t <sub>SUHXTL</sub>	HXTAL oscillator startup time	VDD=3.3V, T <sub>A</sub> =25°C, ESR=40Ω, C <sub>HXTL</sub> = 9pF	-	465	-	μs

$t_{SUHXTL}$ Quick	HXTAL oscillator Quick startup time	VDD=3.3V, $T_A=25^\circ\text{C}$ , ESR=40 $\Omega$ , $C_{HXTL}=9\text{pF}$	-	155	-	$\mu\text{s}$
ESR			-	40	-	$\Omega$
$F_{TOLHXTL}$	Frequency tolerance for the crystal	VDD=3.3V, $T_A=25^\circ\text{C}$	-20	-	20	ppm
$PD_{HXTL}$	Drive level	VDD=3.3V, $T_A=25^\circ\text{C}$	-	-	100	$\mu\text{W}$

Table 5-12 LXTAL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$f_{LXTL}$	Low speed crystal oscillator (LXTAL) frequency	VDD=3.3V, $T_A=25^\circ\text{C}$	-	32.768	-	kHz
$I_{DDLXTL}$	LXTAL oscillator operating current	VDD=3.3V, $T_A=25^\circ\text{C}$	0.3	0.45	0.67	$\mu\text{A}$
$t_{SULXTL}$	LXTAL oscillator Normal startup time	VDD=3.3V, $T_A=25^\circ\text{C}$	330	550	1500	ms
$t_{SULXTL}$ Quick	LXTAL oscillator Quick startup time	VDD=3.3V, $T_A=25^\circ\text{C}$	-	125	-	ms
$ESR_{LXTL}$	Equivalent series resistance 6 pF < CL ≤ 9 pF	VDD=3.3V, $T_A=25^\circ\text{C}$	-	70	-	k $\Omega$
$C_{LoadLXTL}$	Crystal load capacitance	VDD=3.3V, $T_A=25^\circ\text{C}$	-	7	-	pF
$PD_{LXTL}$	Drive level	VDD=3.3V, $T_A=25^\circ\text{C}$	-	-	1	$\mu\text{W}$

Table 5-13 32MHz RCH characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$f_{IRC32M}$	Crystal frequency	VDD=3.3V, $T_A=25^\circ\text{C}$	-	32	-	MHz
$ACC_{IRC32M}$	Frequency accuracy	VDD=3.3V, $T_A=-40^\circ\text{C} \sim +105^\circ\text{C}$	-	-	-	%
		VDD=3.3V, $T_A=-20^\circ\text{C} \sim +85^\circ\text{C}$	-	-	-	%
		VDD=3.3V, $T_A=25^\circ\text{C}$	-	±1	-	%
$D_{IRC32M}$	IRC32M oscillator duty cycle	VDD=3.3V, $f_{IRC32M}=32\text{MHz}$ , $T_A=25^\circ\text{C}$	48	50	52	%
$I_{DDIRC32M}$	Operating current	VDD=3.3V, $f_{IRC32M}=32\text{MHz}$ , $T_A=25^\circ\text{C}$	-	82	-	$\mu\text{A}$
$t_{SUIRC32M}$	Startup time	VDD=3.3V, $f_{IRC32M}=32\text{MHz}$ , $T_A=25^\circ\text{C}$	-	5	-	$\mu\text{s}$
$d_{fIRC32M}$	25 $^\circ\text{C}$ , the frequency drifts with the supply voltage	VDD=1.8V~3.6V, $T_A=25^\circ\text{C}$	-	0.5	-	%/V

Table 5-14 32kHz RCL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$f_{IRC32k}$	Crystal frequency	VDD=3.3V, $T_A=25^\circ\text{C}$	-	32	-	kHz
$ACC_{IRC32K}$	Frequency accuracy	VDD=3.3V, $T_A=25^\circ\text{C}$ (After calibration)	-	$\pm 500$	-	ppm
$D_{IRC32K}$	IRC32K oscillator duty cycle	VDD=3.3V, $f_{IRC32K}=32\text{kHz}$ , $T_A=25^\circ\text{C}$	48	50	52	%
$I_{DDIRC32K}$	Operating current	VDD=3.3V, $f_{IRC32K}=32\text{kHz}$ , $T_A=25^\circ\text{C}$	-	310	-	nA
$t_{SUIRC32K}$	Startup time	VDD=3.3V, $f_{IRC32K}=32\text{kHz}$ , $T_A=25^\circ\text{C}$	-	480	-	$\mu\text{s}$
$df_{IRC32K}$	$25^\circ\text{C}$ , The frequency drifts with the supply voltage	VDD=1.8V~3.6V, $T_A=25^\circ\text{C}$	-	1	-	%/V

Table 5-15 DPLL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$f_{PLLIN}$	PLL input clock frequency	VDD=3.3V, $T_A=25^\circ\text{C}$	-	32	-	MHz
$f_{PLL}$	PLL output clock frequency	VDD=3.3V, $T_A=25^\circ\text{C}$	48	48	48	MHz
$I_{PLL}$	Operating current	VDD=3.3V, $T_A=25^\circ\text{C}$	96	105	145	$\mu\text{A}$

## 5.5 ADC characteristics

Table 5-16 Power supply and input range conditions

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$V_{Ax(VBG\ adc)}$	Analog input voltage range, VBG (1.2V)	VDD=3.3V, $T_A=25^\circ\text{C}$	0	-	1.2	V
$V_{Ax(VDD)}$	Analog input voltage range, VDD	VDD=3.3V, $T_A=25^\circ\text{C}$	0	-	VDD	V
$I_{ADC}$	ADC supply current	VDD=3.3V, $T_A=25^\circ\text{C}$ $F_{adc}=16\text{MHz}$	-	0.55	-	mA
$C_{sample}$	Internal sample and hold capacitors (PAD and PCB capacitors not included)		-	10	-	pF
$R_{ADC}$	Sampling switch resistance	$0\text{V} \leq V_{Ax} \leq \text{VDD}$	-	300	-	$\Omega$
$R_{In}$	External input impedance, continuous sampling	$0\text{V} \leq V_{Ax} \leq \text{VDD}$	0.86	-	4734.70	k $\Omega$

Table 5-17 ADC built-in voltage reference

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V <sub>BGADC</sub>	Internal 1.2V Reference Voltage	VDD=3.3V, T <sub>A</sub> =25°C	1.1	1.2	1.3	V
T <sub>Coef</sub>	Temperature factor	T <sub>A</sub> =-40°C~105°C; VDD=1.8V~3.6V	-	30	-	ppm/°C

Table 5-18 Time parameters

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
F <sub>ADC</sub>	ADC clock frequency	VDD=3.3V, T <sub>A</sub> =25°C	4	16	24	MHz
T <sub>S</sub>	Sample time	VDD=3.3V, T <sub>A</sub> =25°C	4	1539	8192	1/F <sub>adc</sub>
T <sub>CONV</sub>	Conversion time	VDD=3.3V, T <sub>A</sub> =25°C	32	1580	8298	1/F <sub>adc</sub>

Table 5-19 Linearity parameter

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
INL	Integral linearity error	VDD=3.3V, T <sub>A</sub> =25°C	-	-	±3	LSB
DNL	Differential linearity error	VDD=3.3V, T <sub>A</sub> =25°C	-	-	±2	LSB
SNR	Signal to Noise Ratio	F <sub>adc</sub> = 16MHz Input Clock 250kHz VDD=3.3V, T <sub>A</sub> =25°C	-	64.3	-	dB
THD	Total harmonic distortion		-	75	-	dB
SFDR	Spurious-free signal dynamic range		-	77.29	-	dB
ENOB	Effective number of bits		-	10.33	-	Bit

Table 5-20 RIN

ADC significant bit	F <sub>ADC</sub> (MHz)	T <sub>s</sub> (cycles)	T <sub>s</sub> (us)	R <sub>inmax</sub> (kΩ)
12	32	4	0.125	0.86
12	32	8	0.25	2.01
12	32	32	1	8.95
12	32	64	2	18.20
12	32	128	4	36.69
12	32	8192	256	2367.20
12	16	4	0.25	2.01
12	16	8	0.5	4.32
12	16	32	2	18.20
12	16	64	4	36.69
12	16	128	8	73.68



12	16	8192	512	4734.70
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Note: The sampling condition is continuous sampling.

## 5.6 PMU characteristics

Table 5-21 PMU characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V <sub>HLDO</sub>	HLDO output voltage range, external capacitor	VDD=3.3V, T <sub>A</sub> =25°C	1.1	1.2	1.4	V
VDD <sub>PSRR</sub>	Power supply rejection ratio of VDD	VDD=3.3V, T <sub>A</sub> =25°C	-15	-	-	dB

## 5.7 General operating conditions

Table 5-22 General operating conditions

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VDD*	Operating voltage	T <sub>A</sub> =25°C	1.8	-	3.6	V
VIPIO2*	Operating voltage	T <sub>A</sub> =25°C	1.8	-	3.6	V
T <sub>ST</sub>	Storage temperature	-	-65	-	150	°C
T <sub>A</sub>	Ambient temperature	-	-40	-	125	°C
T <sub>J</sub>	Junction temperature	-	-40	-	125	°C
R <sub>θJA</sub>	Thermal resistance	-	-	TBD	-	°C/W

Note: DCDC-OFF

## 5.8 DCDC characteristics

Table 5-23 DCDC characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V <sub>IN_DCDC</sub>	Input voltage range	VDD=3.3V, T <sub>A</sub> =25°C	2	-	3.6	V
V <sub>OUT_DCDC</sub>	Output voltage range	VDD=3.3V, T <sub>A</sub> =25°C	1.2	1.5	2	V
T <sub>EN_DCDC</sub>	Standup time	VDD=3.3V, I <sub>LOAD</sub> =10mA, T <sub>A</sub> =25°C, L <sub>DCR</sub> =80mΩ	-	200	-	us
η	Efficiency	VDD=3.3V, I <sub>LOAD</sub> =10mA, T <sub>A</sub> =25°C, L <sub>DCR</sub> =80mΩ	-	88	-	%
VR <sub>PL_DCDC</sub>	Ripple	VDD=3.3V, T <sub>A</sub> =25°C	-	43	-	mv
I <sub>OUT</sub>	Drive peak current	VDD=3.3V, T <sub>A</sub> =25°C	-	100	-	mA
I <sub>AVG</sub>	Drive average current	VDD=3.3V, T <sub>A</sub> =25°C	-	30	-	mA
L <sub>DCDC</sub>	Effective inductance	VDD=3.3V, T <sub>A</sub> =25°C	-	2.2	-	μH
C <sub>OUT_DCDC</sub>	Effective load capacitance	VDD=3.3V, T <sub>A</sub> =25°C	1	4.7	-	μF
F <sub>osc_DCDC</sub>	Oscillation frequency	VDD=3.3V, T <sub>A</sub> =25°C	-	-	1000	kHz

## 5.9 ESD characteristics

Table 5-24 ESD characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VESDHBM <sup>[1]</sup>	ESD @ Human Body Mode	T <sub>A</sub> =25°C	-	±4	-	kV
VESDCDM <sup>[2]</sup>	ESD @ Charge Device Mode	T <sub>A</sub> =25°C	-	±2000	-	V
VESDMM <sup>[3]</sup>	ESD @ machine Mode	T <sub>A</sub> =25°C	-	±200	-	V
I <sub>latchup</sub> <sup>[4]</sup>	Latch up current	T <sub>A</sub> =25°C	-	±500	-	mA

Notes:

1. Determined by ANSI/ESDA/JEDEC JS-001 standard, Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) - Device Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 Electrostatic Discharge Sensitivity (ESD) Test Standard.
3. Determined according to JESD22-A115-C electrostatic discharge sensitivity (ESD) test standard.
4. Determined according to JEDEC EIA/JESD78 standard.

## 5.10 Absolute maximum ratings

Table 5-25 Absolute maximum ratings

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VDD - VSS	Supply voltages	T <sub>A</sub> =25°C	-0.3	-	3.6	V
VIN	I/O pin voltage	T <sub>A</sub> =25°C	VSS-0.3	-	VDD + 0.3	V
PVDD	Extreme power consumption	VDD=3.3V, T <sub>A</sub> =25°C DCDC power supply	-	-	TBD	mW

## 5.11 MCU current characteristics

Symbol	Parameter	Conditions	DCDC OFF		DCDC ON
			Typ(mA)	Typ(mA)	Typ(mA)
Run mode	All peripherals clock on, run while(1) in flash	System clock source: RCH (.cal 32M)	4M	0.91	0.686
			8M	1.3	0.916
			16M	2.09	1.36
			32M	3.77	2.28
		System clock source: XTH (.off rch)	4M	1.42	0.985
			8M	1.81	1.2
			16M	2.61	1.64
			32M	4.29	2.54
		System clock source: DPLL	6M	1.56	1.05
			12M	2.15	1.38

		(.ref rch(.cal 32M))	24M	3.4	2.05
		(.base 48M)	48M	5.71	3.44
		System clock source:	6M	2.08	1.34
		DPLL	12M	2.69	1.67
		(.ref xth)	24M	3.95	2.34
		(.base 48M) (.off rch)	48M	6.18	3.57
		System clock source:	4M	1.39	0.953
		DPLL	8M	1.78	1.17
		(.ref rch(.cal 32M))	16M	2.58	1.61
		(.base 64M)	32M	4.27	2.51
		System clock source:	4M	1.9	1.25
		DPLL	8M	2.3	1.46
		(.ref xth)	16M	3.13	1.91
		(.base 64M) (.off rch)	32M	4.85	2.82
	All peripherals clock off, run while(1) in flash	System clock source: RCH (.cal 32M)	4M	0.736	0.523
			8M	0.943	0.719
			16M	1.37	0.963
			32M	2.23	1.43
		System clock source: XTH (.off rch)	4M	0.945	0.723
			8M	1.15	0.84
			16M	1.57	1.07
			32M	2.42	1.54
		System clock source: DPLL (.ref rch(.cal 32M)) (.base 48M)	6M	1.01	0.747
			12M	1.32	0.921
			24M	1.96	1.25
			48M	3.29	2.00
		System clock source: DPLL (.ref xth) (.base 48M) (.off rch)	6M	1.22	0.903
			12M	1.54	1.05
24M	2.19		1.41		
48M	3.54		2.12		
System clock source: DPLL (.ref rch(.cal 32M)) (.base 64M)	4M	0.925	0.693		
	8M	1.14	0.818		
	16M	1.56	1.05		
	32M	2.43	1.53		
System clock source: DPLL (.ref xth) (.base 64M) (.off rch)	4M	1.14	0.831		
	8M	1.35	0.947		
	16M	1.78	1.18		
	32M	2.66	1.66		

Notes: Test conditions - DVDD=1.2V, VDD=3.3V, VBG=1.2V, T<sub>A</sub>=25°C

Symbol	Parameter	Conditions		Typ(μA)	
standby m0	wake by gpio			0.28	
Symbol	Parameter	Conditions	Clk source	Typ(μA)	
standby m1	wake by 32k timer	sw=0x0d (Note 1)	XTL	1.88(Note 3)	
		sw=0x1f (Note 1)	XTL	2.18(Note 3)	
	wake by gpio	sw=0x0d (Note 1)		1.32(Note 3)	
		sw=0x1f (Note 1)		1.63(Note 3)	
	wake by wdt	sw=0x0d (Note 1)	XTL	1.85(Note 3)	
		sw=0x1f (Note 1)	XTL	2.18(Note 3)	
	wake by lvr	sw=0x0d (Note 1)		2.05(Note 3)	
		sw=0x1f (Note 1)		2.42(Note 3)	
	wake by bod	sw=0x0d (Note 1)		2.11(Note 3)	
		sw=0x1f (Note 1)		2.48(Note 3)	
	Deepsleep	wake by 32k timer	sw=0x0d (Note 1)	XTL	2.96(Note 3)
			sw=0x1f (Note 1)	XTL	3.37(Note 3)
wake by gpio		sw=0x0d (Note 1)		2.46(Note 3)	
		sw=0x1f (Note 1)		2.86(Note 3)	
wake by wdt		sw=0x0d (Note 1)	XTL	2.99(Note 3)	
		sw=0x1f (Note 1)	XTL	3.37(Note 3)	
wake by peripheral timer		sw=0x0d (Note 1)	XTL	4.03(Note 3&4)	
		sw=0x1f (Note 1)	XTL	4.73(Note 3)	
wake by 32k timer		sw=0x0d (Note 1)	XTL*	4.06(Note 3&4)	
		sw=0x1f (Note 1)	XTL*	4.69(Note 3)	
Sleep		wake by gpio	LDO all peripheral clocks on		4620
			LDO non-essential peripheral clocks off		1820
	DCDC all peripheral clocks on			2700	
	DCDC non-essential peripheral clocks off			1210	

Note: Test conditions - DVDD=1.2V, VDD=3.3V, VBG=1.2V, TA=25°C, DCDC ON

Note\*: PWM output enable.

Notes:

1. The *sw* indicates the module control switch for PAN101x power retention in low-power mode, bit 1 for power retention, bit 0 for power down, 0d = sram32k+phy\_sram+cpu\_retention, 1f = all\_sram\_retention
2. In LPLDOH Enhance mode, the *lpldoh* voltage is affected by *lpldoh* trim and *vref* trim, where *vref* trim compensates *lpldoh* when *lpldoh* jitter, so that it does not fall to the voltage of *vref* trim as much as possible.
3. In LPLDOH mode2, the *lpldoh* trim voltage does not take effect, and the effective voltage is the *vref\_trim* voltage. The *lpldoh* undershoot does not occur in this mode, and the bottom current is reduced.
4. PWM can output waveforms normally in *Deepsleep* mode, but only in *Deepsleep* mode2, and see Note 5 for instructions on *Deepsleep* mode2.
5. When the register *LP\_FL\_CTRL* [31] is 1, the switch between LPLDOL and LPLDOH is connected, and LPLDOL enable is off. LPLDOH supplies power to LPLDOL. This is the mode 2. Mode 2 power consumption increases.

## 6 Application Reference Diagram

Please visit the following address for the latest **Application Reference Diagram** and **hardware design notes**: [PAN10xx Hardware Reference Design Guide](#)

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## 7 Package Dimensions

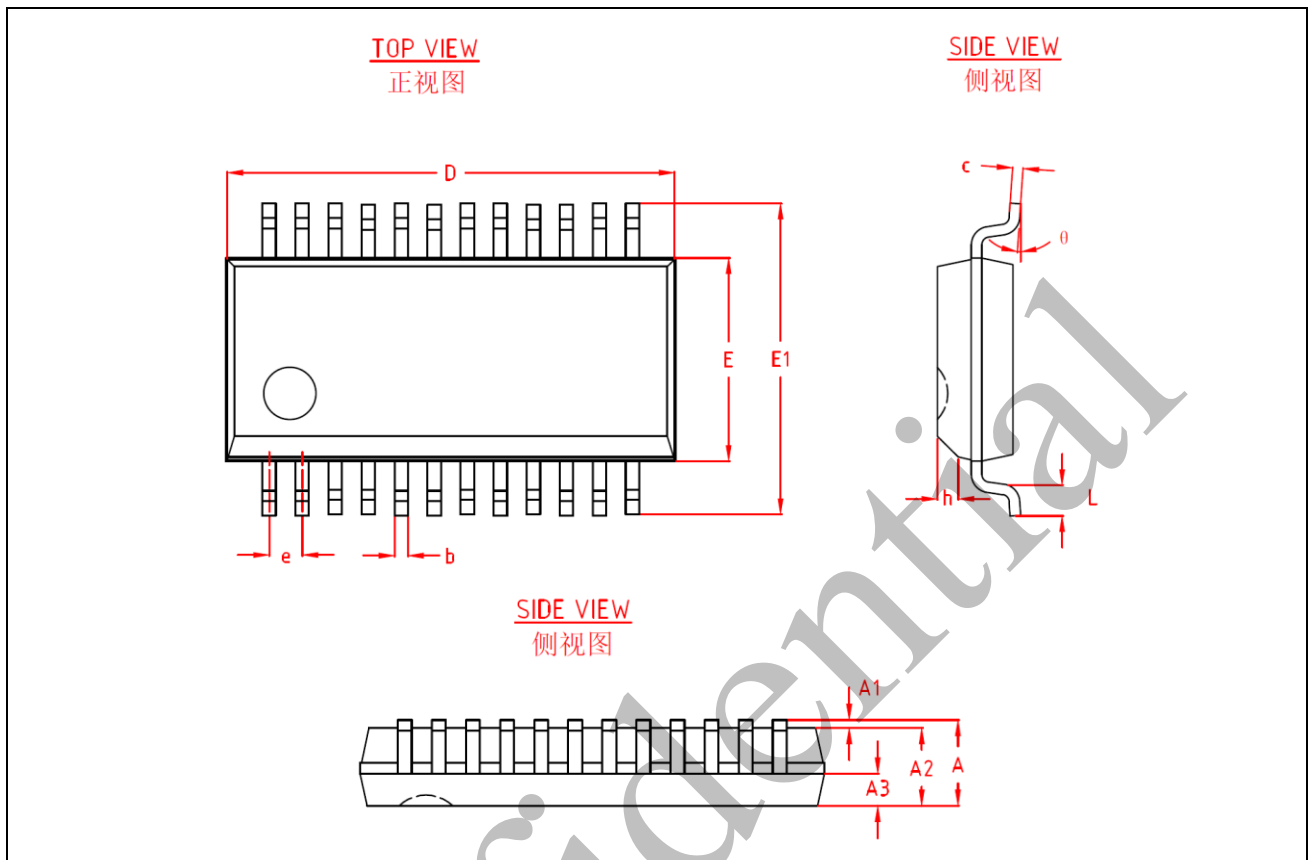


Figure 7-1 Package View for SSOP24

Table 7-1 Package Dimension for SSOP24

SYMBOL	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.75
A1	0.10	-	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.23	-	0.31
c	0.19	-	0.25
D	8.50	8.60	8.70
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	0.635BSC		
h	0.30	-	0.50
L	0.40	-	0.80
Ø	0	-	8°

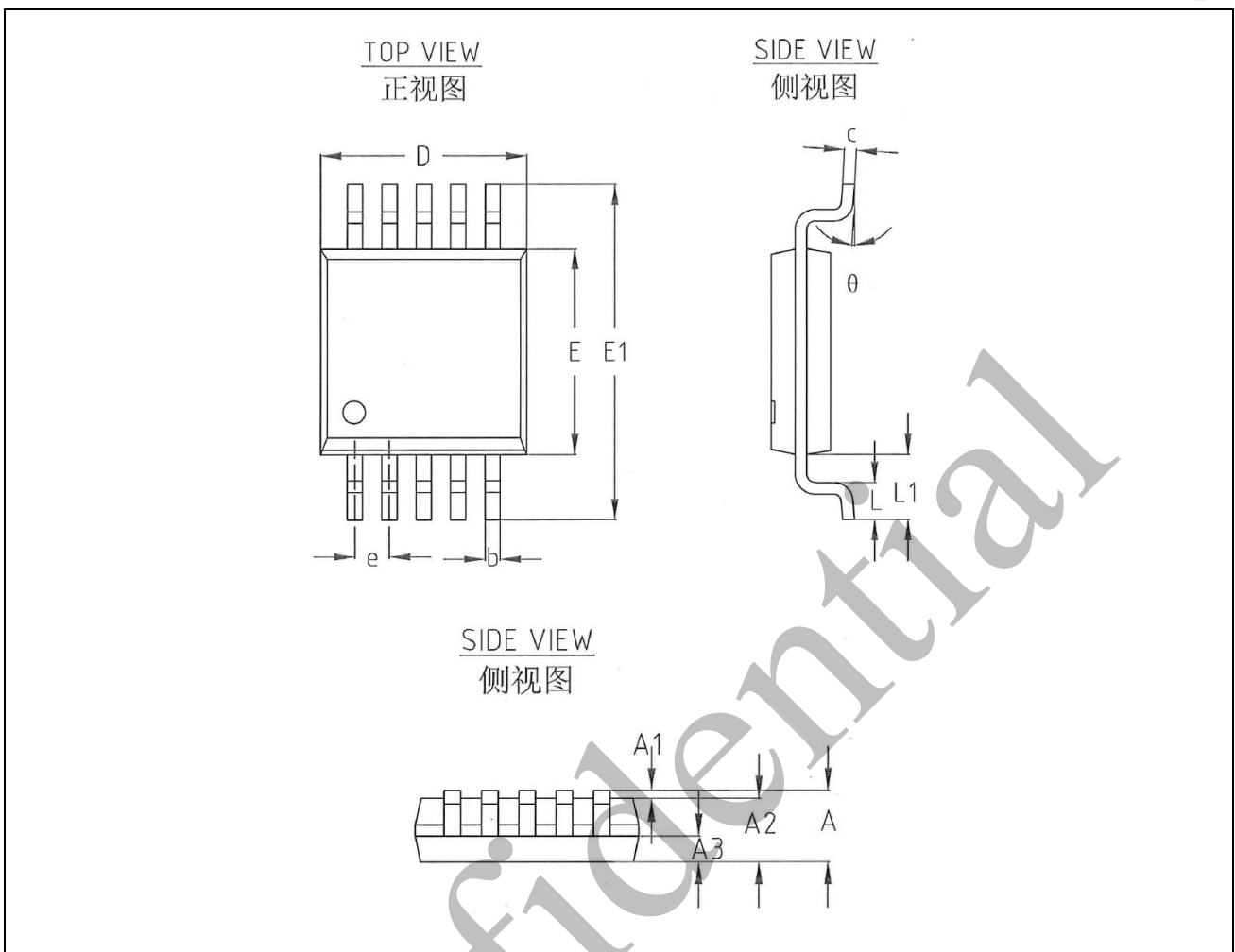


Figure 7-2 Package View for MSOP10

Table 7-2 Package Dimension for MSOP10

SYMBOL	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.10
A1	0.05	-	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18	-	0.26
c	0.15	-	0.19
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
e	0.50BSC		
L	0.40	-	0.70
L1	0.95REF		
∅	0	-	8°

## Abbreviation

<b>A</b>		FCR	FIFO Control Register
APB	Advanced Peripheral Bus	FIFO	First Input First Output
ADC	Analog-to-Digital Converter	FMC	Flash Memory Controller
ALT	Alternate Function Select		The longest time that the HiSilicon product is allowed to remain in the workshop (environ-ment <30 °C / 60% RH, before unpacking the moisture-proof packaging to reflow).
ANAC	Analog Control	Floor life	
APROM	Application ROM		
ATT	Attribute Protocol		
<b>B</b>		<b>G</b>	
BAUDR	Baud Rate Select Register	GAP	Generic Access Profile
BLDC	Brushless Direct Current Motor	GATT	Generic Attribute Profile
Bluetooth LE	Bluetooth Low Energy	GPIO	General-purpose I/O
BOD	Brown-out Detector	<b>H</b>	
BOM	Bill of Materials	HCLK	Tstem Clock
<b>C</b>		HIC	Humidity Indicator Card
CFGx	Configuration Register for Channel x	HID	Human Interface Device
ChEnReg	DMA Channel Enable Register	HIRC	32MHz internal high speed oscillator
CMPDAT	Compare value	HTX	Halt TX
CPU	Central Processing Unit	HXT	32MHz external high speed crystal oscillator
CRC-32	Cyclic Redundancy Check	<b>I</b>	
CTLx	Control Register for Channel x	I2C	Inter-Integrated Circuit
CTRLR0	Control Register 0	IAP	In-Application-Programming
CTRLR1	Control Register 1	ICE	In-Circuit-Emulator
<b>D</b>		ICP	In-Circuit Programming
DARx	Destination Address Register for Channel x	ICR	Interrupt Clear Register
Desiccant	A material for adsorbing moisture while remaining dry	IDR	Identification Register
DFBA	Data Flash Base Address Register	IER	Interrupt Enable Register
DLF	Divisor Latch Fraction Register	IIR	Interrupt Identity Register
DLH	Divisor Latch High	IMR	Interrupt Mask Register
DLL	Divisor Latch Low	IRSR	Interrupt Raw Status Registers
DmaCfgReg	DMA Configuration Register	ISB	Instruction Synchronization Barrier
DMACR	DMA Control Register	ISP	In-System Programming
DmaIdReg	DMA ID Register	ISR	Interrupt Service Routine
DMARDLR	DMA Receive Data Level Register	<b>L</b>	
DMASA	DMA Software Acknowledge	L2CAP	Logical Link Control and Adaptation Protocol
DMATDLR	DMA Transmit Data Level Register	LCR	Line Control Register
DR	Data Register	LCR_EXT	Line Extended Control Register
DSTATARx	Destination Status Address Register for Channel x	LDO	Low dropout regulator
DSTATx	Destination Status Register for Channel x	LDR0M	Loader ROM
<b>E</b>		LIRC	32 kHz internal low speed RC oscillator
ESD	Electro-Static discharge	LNA	Low Noise Amplifier
<b>F</b>			



LSB	Least significant bit		Clear Register
LSR	Line Status Register		Receive FIFO Underflow Interrupt
LstDstReg	Last Destination Transaction Request Register	RXUICR	Clear Register
LstSrcReg	Last Source Transaction Request Register	<b>S</b>	
LVR	Low Voltage Reset	SARx	Source Address Register for Channel x Register
LXT	32.768 kHz external low speed crystal oscillator	SCB	System Control Block Registers
<b>M</b>		SCB	System Control Block Registers
MBB	Moisture Barrier Bag	SCR	Scratchpad Register
MCR	Modem Control Register	SER	Slave Enable Register
MCU	Micro Control Unit	SglReqDstReg	Single Destination Transaction Request Register
MDM	Mobile Device Management	SglReqSrcReg	Single Source Transaction Request Register
MFP	Multiple Function Port	Shelf Life	Normal storage time after moisture-proof packaging
MISO	Master input slave output	SM	Security Manager
MOSI	Master output slave input	SoC	System on chip
MSB	Most Significant Bit	SPI	Serial Peripheral Interface
MSL	Moisture sensitivity level, this product is on level 3	SPROM	Security protection ROM
MSR	Modem Status Register	SR	Status Register
MSTICR	Multi-Master Interrupt Clear Register	SRAM	Static random access memory
<b>N</b>		SSTATARx	Source Status Address Register for Channel x
NMI	Non Maskable Interrupt	SSTATx	Source Status Register for Channel x
NVIC	Nested Vectored Interrupt Controller	Statusint	Combined Interrupt Status Register
<b>P</b>		SWD	Serial Wire Debug
PA	Power Amplifier	SysTick	System Timer
PLL	Phase Locked Loop	<b>T</b>	
POR	Power-on Reset	TAR	Transmit Address Register
PWM	Pulse Width Modulation	TFL	Transmit FIFO Level
<b>R</b>		THR	Transmit Holding Register
RAR	Receive Address Register	THRE	Transmitter Holding Register Empty
RBR	Receive Buffer Register	TMR	Timer Controller
ReqDstReg	Destination Software Transaction Request Register	TXFLR	Transmit FIFO Level Register
ReqSrcReg	Source Software Transaction Request Register	TXFTLR	Transmit FIFO Threshold Level Register
RF	Radio frequency	TXOICR	Transmit FIFO Overflow Interrupt Clear Register
RFL	Receive FIFO Level	<b>U</b>	
RISR	Raw Interrupt Status Register	UART	Universal Asynchronous Receiver/Transmitters
ROM	Read-Only Memory	USR	UART Status Register
RSSI	Received Signal Strength Indication	<b>W</b>	
RTOS	Real Time Operating System	WDT	Watchdog Timer
RXFLR	Receive FIFO Level Register	WWDT	Window Watchdog Timer
RXFTLR	Receive FIFO Threshold Level Register		
RXOICR	Receive FIFO Overflow Interrupt		

## Revision History

Version	Date	Content
1.0	Apr. 2024	Initial
1.1	Apr. 2024	Update the Application Reference Diagram.
1.2	May. 2024	Update the Electrical specification.
1.3	Jun. 2024	Update the Bluetooth Features.
1.4	Aug. 2024	Add the MSOP10.
1.5	Nov. 2024	Update the Application Reference Diagram. Update the Table 5-7. Update the Typ value of <i>standby ml</i> in the MCU current characteristics.
1.6	Dec. 2024	Update the Table 5-7. Update the Pin Information.

Internal version, for reference only.

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