PANCHIP

PAN108 series

Datasheet

V2.9 Dec 2024

Panchip Microelectronics Co., Ltd.

BLE SoC Transceiver

General Description

PAN108 series integrates BLE5.3 and 2.4GHz dual-mode wireless SoC transceiver. The wireless transceiver circuit works in the 2.400-2.483GHz universal ISM frequency band. There is an external 512KB/1MB Flash program memory and a built-in 64KB SRAM memory. In addition, PAN108 series is equipped with a wealth of peripherals, including up to 48 GPIOs, 24-channel PWM, three 32-bit timers, 1 I2C, 2 UARTs, 2 SPIs, 8 external channels ADC, WDT, WWDT, I2S master, I2S slave, USB2.0(Full Speed), 32K RC automatic calibration, QDEC and automatic key-scan, etc. PAN108 series is suitable for wireless mouse and keyboard, smart home and elec-tronic shelf label, BLE-AOA indoor locating.

Key Features

- **MCU**
  - 32-bit MCU core running up to 64MHz
- **Memory**
  - Build-in 512KB/1MB flash supporting deep sleep mode
  - 64KB SRAM
  - 256B eFuse
  - 4 KB cache
- **Low Power**
  - Active mode RX: 5.6mA(DCDC)
  - Active mode TX at 0dBm: 6.1mA(DCDC)
  - Standby mode : 0.34uA
  - Standby mode(SRAM retention): 2uA(GPIO, XTL, RCL can wake up)
  - Deep sleep mode: 8uA(All Logic Retention, GPIO, XTL, RCL can wake up)
- **Clock**
  - 32MHz RC
  - 32MHz XTAL
  - 32kHz RC
  - 32.768kHz XTAL
  - DPLL(Two channels: 64MHz/48MHz and 48MHz (USB 2.0))
- **RF**
  - Mode
    - BLE5.3 modes: 1Mbps, 2Mbps, 500kbps, 125kbps
    - 2.4G private protocol: 1Mbps / 2Mbps, supporting hardware ACK
  - Output power: -45dBm~7dBm
  - Receiver
    - -100dBm@125kbps
    - -99dBm@500kbps
    - -96dBm@1Mbps
    - -93dBm@2Mbps
  - RSSI
    - Resolution: 0.25dB
    - Accuracy: ±2dB
    - Range: - 90dbm ~ -15dBm
  - Positioning: AoA/AoD supported
  - Single antenna supported
  - Safety regulations: BQB / ETSI / FCC
- **Peripheral**
  - Up to 48 GPIOs (there are two power supply voltages)
  - 24-channel PWM
  - Three 32-bit timer
  - One I2C
  - Two UARTs
  - Two SPIs
  - 3-channel DMA
  - 11-channel ADC(8 ext, bandgap, VDD/4, temp)
  - Two I2S(one I2S master and one I2S slave)
  - 3-channel QDEC
  - WDT / WWDT
  - ECC accelerator
  - Automatic key-scan
  - IO / BOD / POR / LVR / System reset
  - FMC(Support IAP, support the boot loader with address 0x0)
  - Clock measurement and clock calibration
  - USB2.0(Full_speed)
  - Flash data encryption
  - RTC (Real Time Counter)
- **Temperature sensor**
  - Support temperature sensor
  - Test range: -40℃ ~ 85℃
  - Accuracy: ±2℃ (With calibration)
- **Power Management**
  - Integrated voltage regulator
  - Operating voltage: 1.8V to 3.7V (Support DCDC)
- **Package**
  - LQFP64 (7×7mm)
  - QFN48 (6×6mm)
  - QFN32 (5×5mm / 4×4mm)
- **Operating Condition**
  - Operating temperature: -40℃ ~ 85℃ / -40℃ ~ 125℃ / -40℃ ~ 105℃
  - Storage temperature: -60℃~150℃
  - ESD
    - HBM: ±2.5kV(LQFP64) / ±5kV(QFN48)/ ±4kV(QFN32)
    - MM: ±250V(LQFP64) / ±250V(QFN48)/ ±300V(QFN32)
    - CDM: ±500V
  - Latch-up: ±500mA

Typical Applications

- High-precision BLE-AOA in-door location system
- Electronic Shelf Label
- Wireless mouse and keyboard
- LED light control

Bluetooth Features

Bluetooth Low Energy Controller

The PAN108 series Bluetooth Low Energy Controller supports all low-energy features required by Bluetooth specification version 5.3. The controller supports the following:

- **Support 1M PHY, 2M PHY and Coded PHY (s2 and s8)**
- **Support Advertising, Scanning, Initiating and Connection (both of Central and Periph-eral) role**
- **Up to 10 Link Layer state machines concurrently:**
  - 1 * Passive Scanning
  - 1 * Non-connectable advertising
  - 8 * Any other combinations (Legacy/Extended/Periodic Adverstising, Scanning and Connection)
- **Support LE Features:**
  - LL Encryption
  - LE Data Packet Length Extension
  - LL Privacy
  - Extended Scanner Filter Policies
  - LE Extended and Periodic Adverstising
  - Channel Selection Algorithm #2
  - Constant Tone Extension
- **Support Update Channel Statistics**

Bluetooth Host

- **Generic Access Profile (GAP) with all possible LE roles**
  - Peripheral & Central
  - Observer & Broadcaster
- **GATT (Generic Attribute Profile)**
  - Server (to be a sensor)
  - Client (to connect to sensors)
- **Pairing support, including the Secure Connections feature from Bluetooth 4.2**
- **Non-volatile storage support for permanent storage of Bluetooth-specific settings and data**
- **Clean HCI driver abstraction**
  - 3-Wire (H5) & 5-Wire (H4) UART
  - SPI
  - Local controller support as a virtual HCI driver

Bluetooth Mesh

- **Compatible with Bluetooth SIG Mesh Profile 1.0.1**
- **Support Mesh Provisioning**
- **Provisioner: PB-ADV**
- **Provisionee: PB-ADV, PB-GATT and PB-Remote**
- **Support Mesh Node Feature : Relay, Proxy, Friend, LPN**
- **Support Mesh Models**
  - SIG Models: Config Model, Health Model and Generic Models (Onoff and Light Con-trol Models)
  - SIG Developing Models: PB-Remote Model and SIG OTA Model
- **Support multiple smart speakers control concurrently for BaiDu Xiaodu, Alibaba Ali-genie and Amazon Echo**
- **Support network control: HeartBeat, Subnet, Secure Beacon and Group Control**
- **Support switch control for over 256 nodes without delay**
- **Mesh Security**
  - Provisioning: FIPS P-256 Elliptic Curve
  - Message: AES-CCM Encryption
  - Network: SEQ Control, IV Index and Key Fresh

Proprietary Radio 2.4G Features

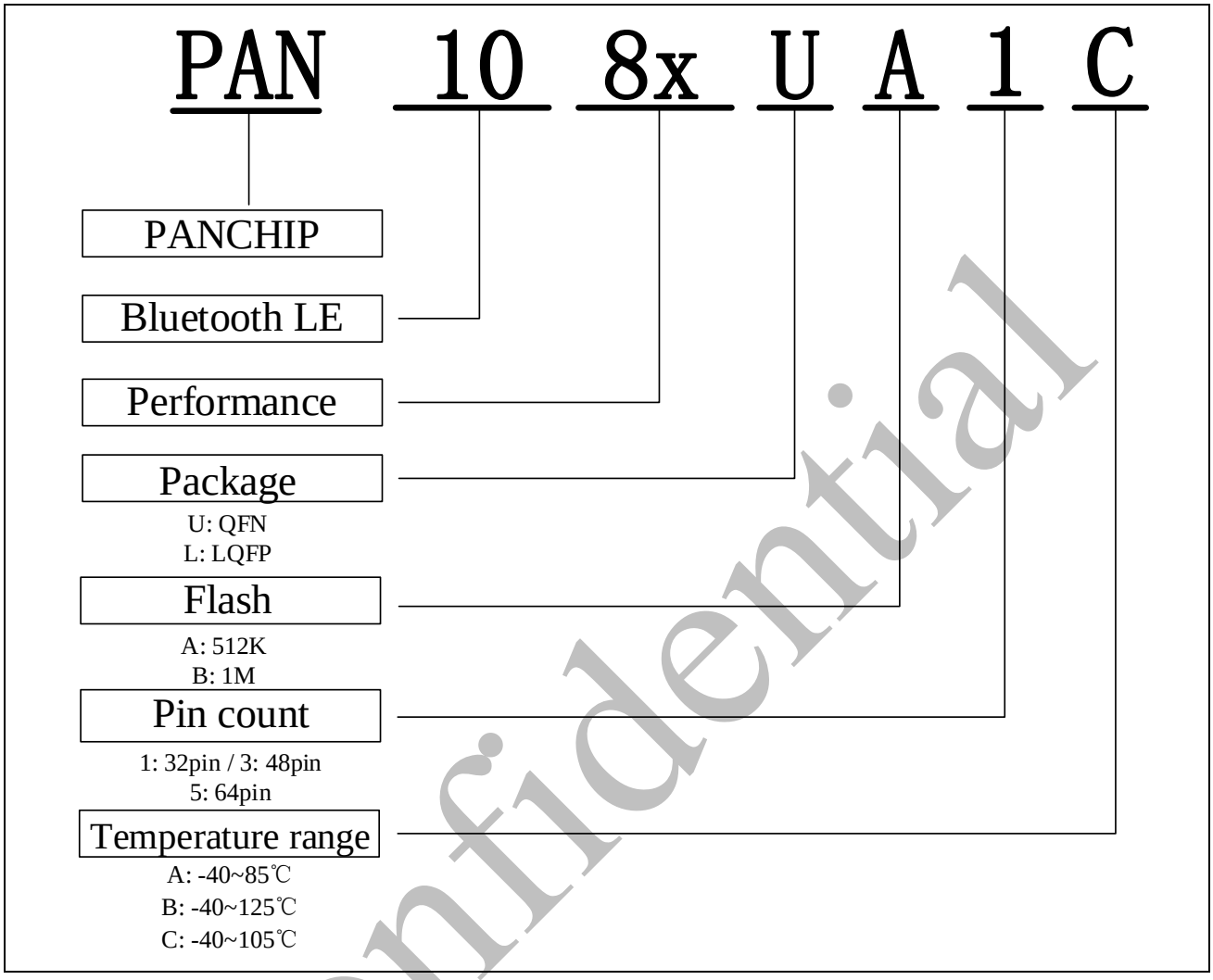
- Support 1M and 2M PHY
- XN297L,PAN1026 Transceiver protocol compliant
- Support No Acknowledge, Acknowledge and Acknowledge with payload
- Support CRC8, CRC16 and CRC24
- Support whitening

Content

List of Tables

List of Figures

1 Naming rule



2 Order information

Part number	Type	Max Clock Frequency	AoA	Pack-age	Pin Count	IO	FLASH	RAM	Temperature Range	Packing
PAN1080 LA5A	BLE5.3	48MHz	○	LQFP (7×7)	64	48	512K	64K	-40~85℃	Tray
PAN1080 LB5A	BLE5.3	64MHz	○	LQFP (7×7)	64	48	1M	64K	-40~85℃	Tray
PAN1080 LB5B	BLE5.3	64MHz	○	LQFP (7×7)	64	48	1M	64K	-40~125℃	Tray
PAN1080 UA3C	BLE5.3	48MHz	○	QFN (6×6)	48	37	512K	64K	-40~105℃	Tape & Reel
PAN1080 UB1A	BLE5.3	64MHz	○	QFN (5×5)	32	21	1M	64K	-40~85℃	Tape & Reel
***PAN1081 UB1A**	BLE5.3	64MHz	○	QFN (5×5)	32	21	1M	64K	-40~85℃	Tape & Reel
PAN1082 UA1C	BLE5.3	48MHz	×	QFN (5×5)	32	21	512K	64K	-40~105℃	Tape & Reel
PAN1083 UA1C	BLE5.3	48MHz	×	QFN (4×4)	32	20	512K	64K	-40~105℃	Tape & Reel

○: Support ×: Not support

*Support sports health protocol

Before ordering, please contact the sales window for the latest mass production information.

3 Block Diagram

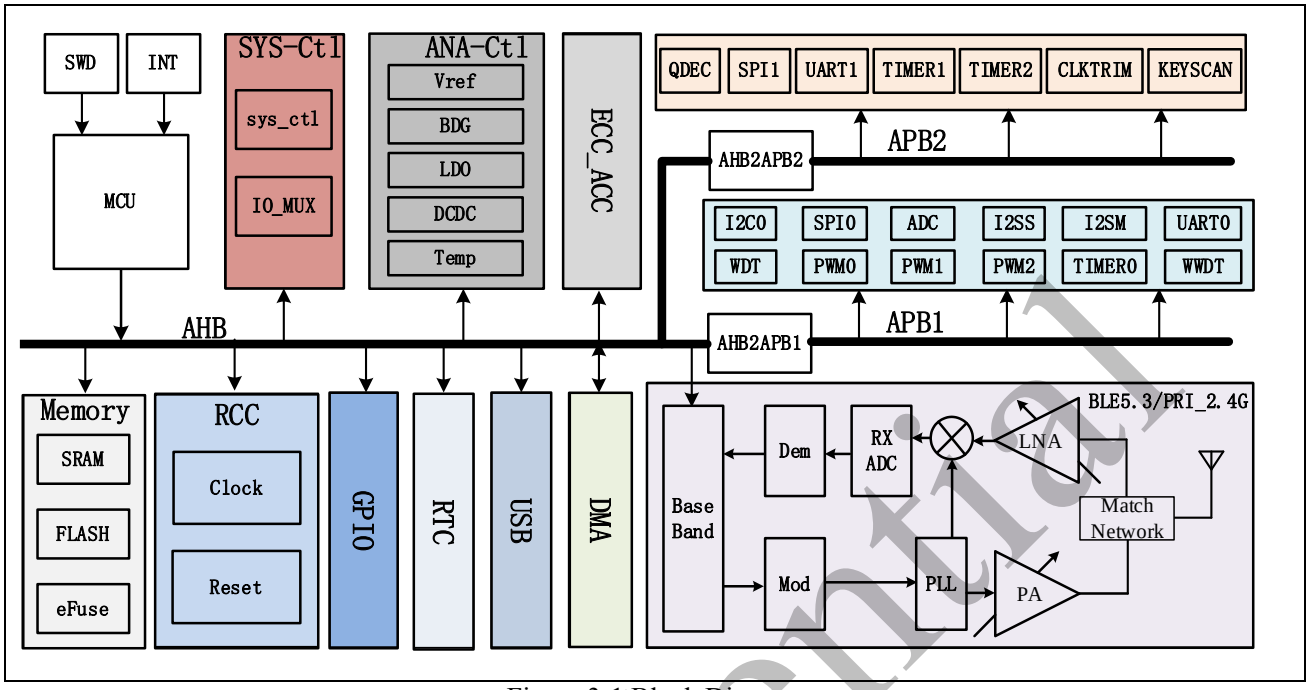


Figure 3-1 Block Diagram

4 Pin Information

4.1 QFN 32-PIN Diagram

PAN1080UB1A / PAN1081UB1A / PAN1082UA1C

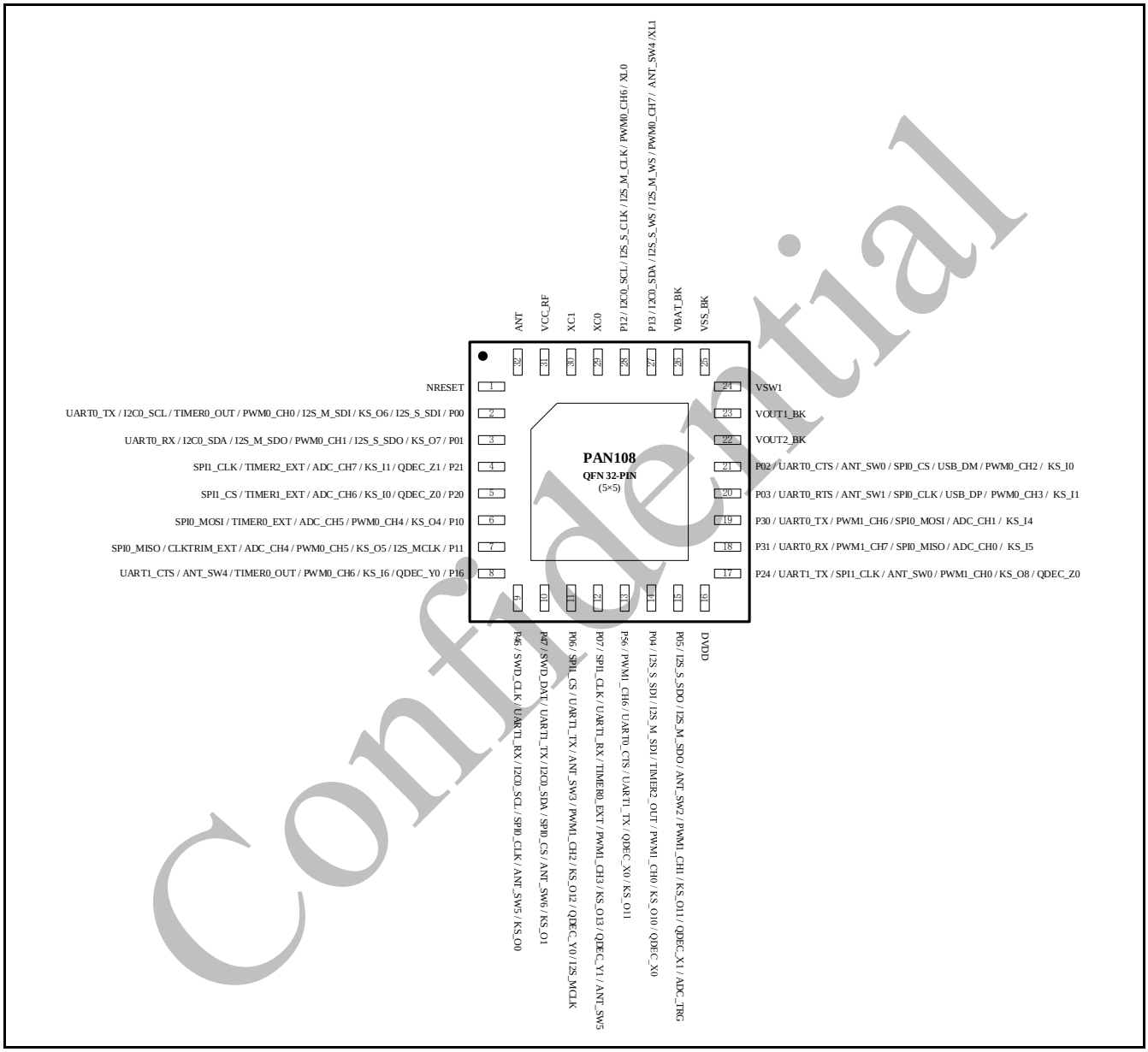


Figure 4-1 QFN 32-PIN (5×5) Diagram

PAN1083UA1C

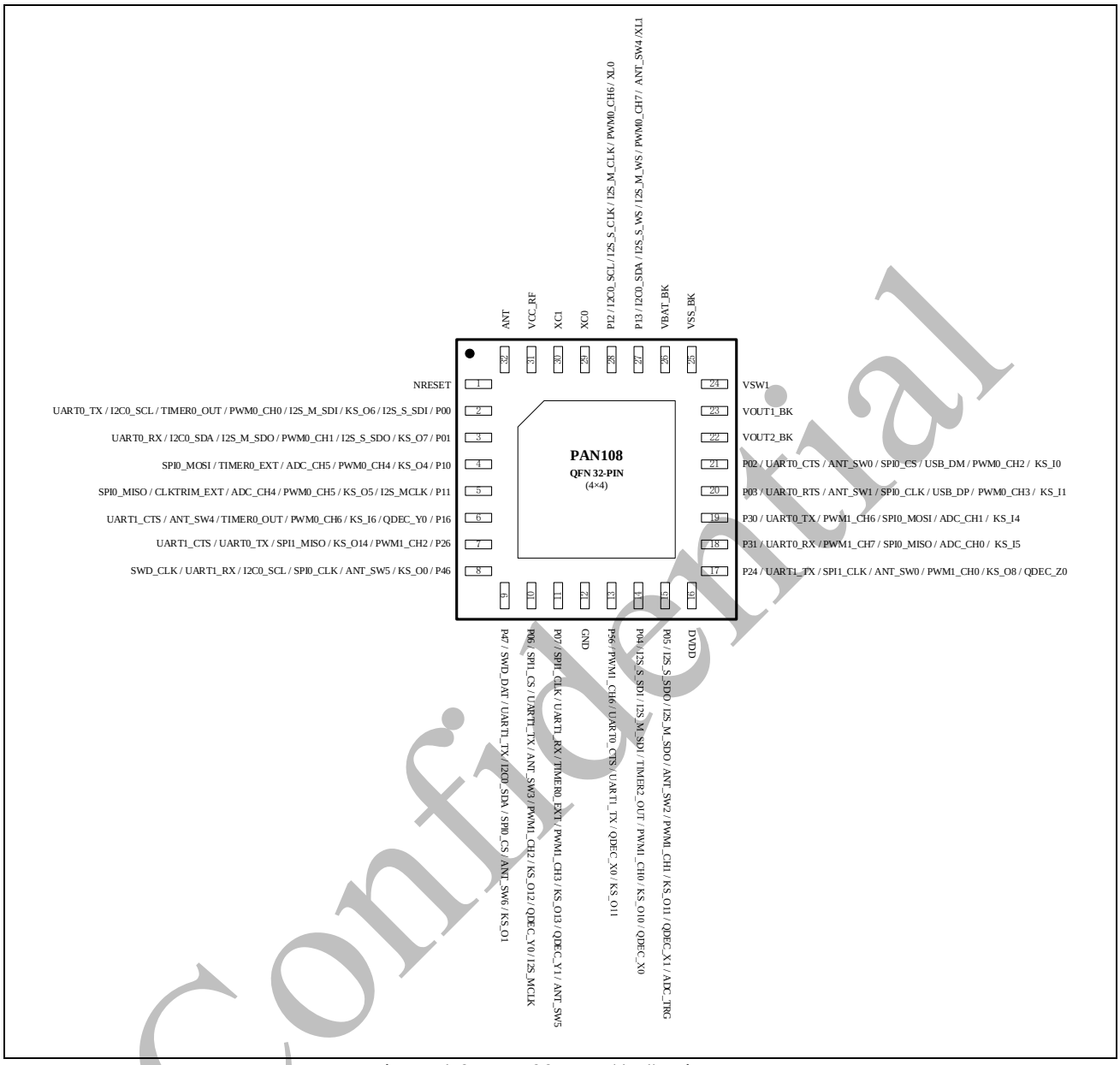


Figure 4-2 QFN 32-PIN (4×4) Diagram

4.2 QFN 48-PIN Diagram

PAN1080UA3C

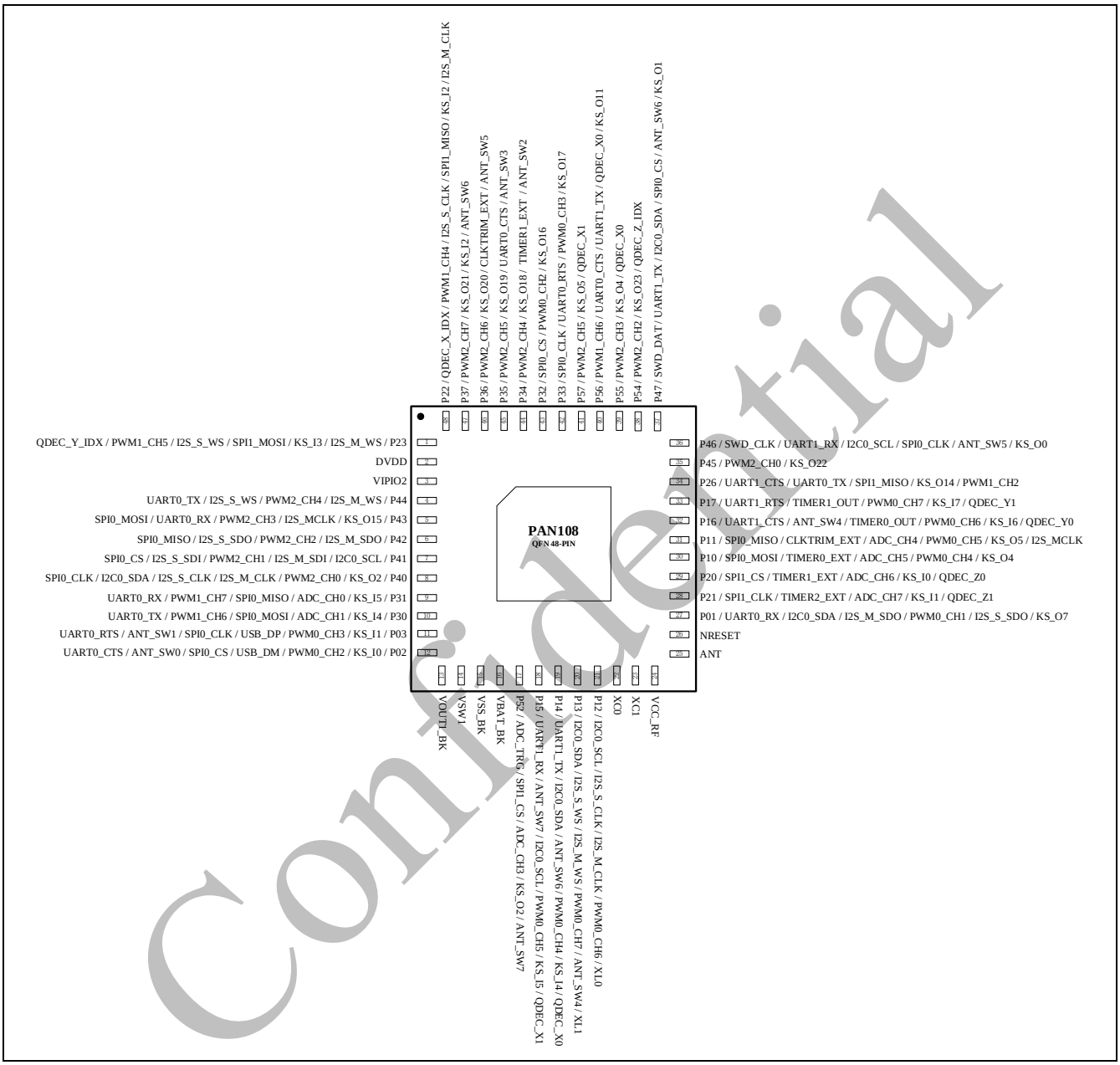


Figure 4-3 QFN 48-PIN Diagram

4.3 LQFP 64-PIN Diagram

PAN1080LA5A / PAN1080LB5A / PAN1080LB5B

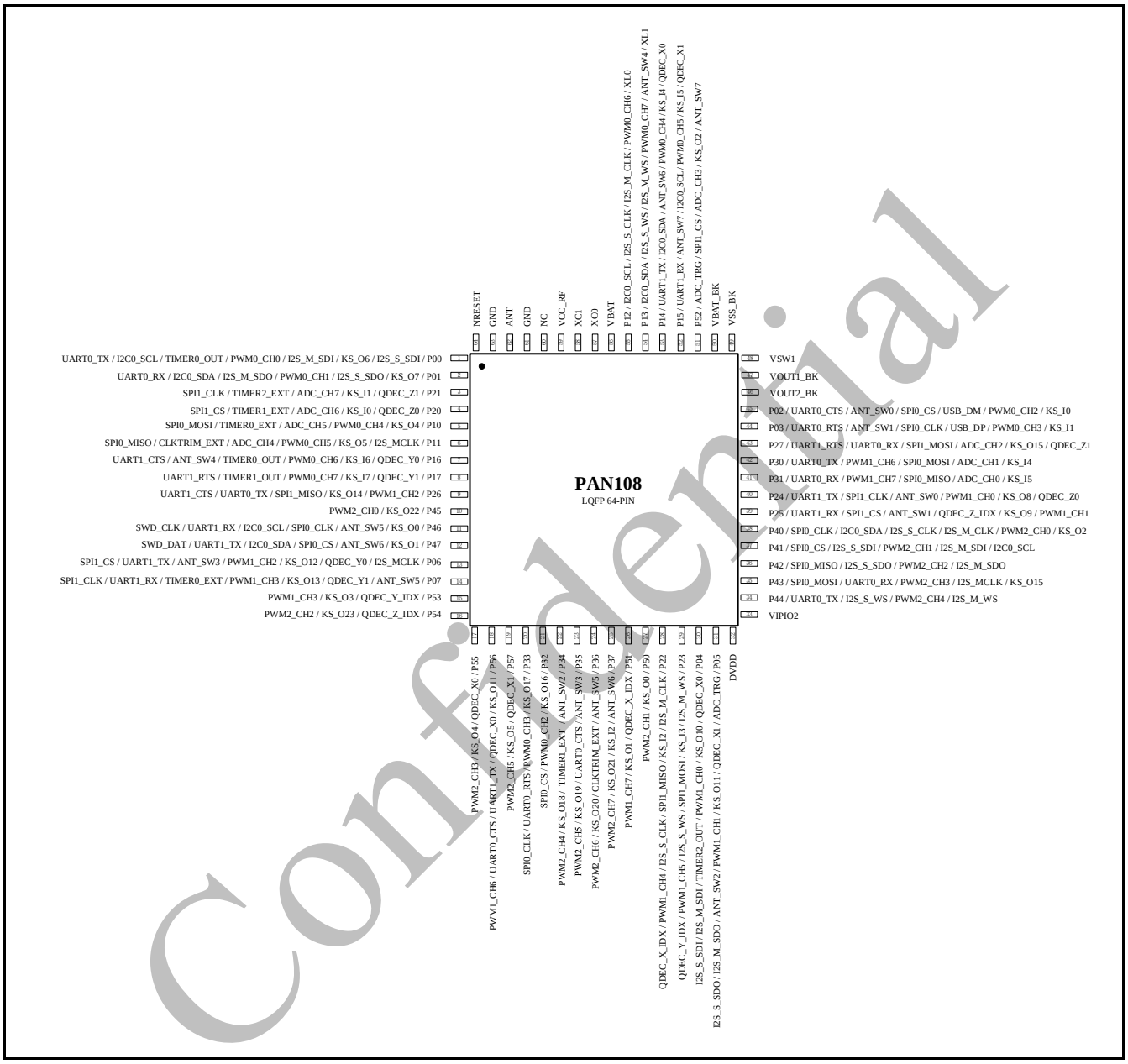


Figure 4-4 LQFP 64-PIN Diagram

4.4 Pin Descriptions

Detail pin descriptions see Table 4-1.

Table 4-1 Pin Descriptions

Package				Pin Name	Pin Type	Description
QFN32 (5×5)	QFN32 (4×4)	QFN48	LQFP64			
2	2	-	1	P00	I/O	General-purpose digital input and output pin
				UART0_TX	O	Uart0 tx pin
				I2C0_SCL	I/O	I2c0 clock pin
				TIMER0_ OUT	O	Timer0 output pin
				PWM0_CH0	O	Pwm0 channel 0 output pin
				I2S_M_SDI	I	I2s master data input pin
				KS_O6	O	Keyscan output channel 6 pin
				I2S_S_SDI	I	I2s slave data input pin
3	3	27	2	P01	I/O	General-purpose digital input and output pin
				UART0_RX	I	Uart0 rx pin
				I2C0_SDA	I/O	I2c0 data pin
				I2S_M_SDO	O	I2s master data output pin
				PWM0_CH1	O	Pwm0 channel 1 output pin
				I2S_S_SDO	O	I2s slave data output pin
				KS_O7	O	Keyscan output channel 7 pin
4	-	28	3	P21	I/O	General-purpose digital input and output pin
				SPI1_CLK	I/O	Spi1 clock pin
				TIMER2_EXT	I	Timer2 external input pin
				ADC_CH7	AI	Adc channel 7 pin
				KS_I1	I	Keyscan input channel 1 pin
				QDEC_Z1	I	Qdec z input channel 1 pin
5	-	29	4	P20	I/O	General-purpose digital input and output pin
				SPI1_CS	I/O	Spi1 cs pin
				TIMER1_EXT	I	Timer1 input pin
				ADC_CH6	AI	Adc channel 6 pin
				KS_I0	I	Keyscan input channel 0 pin
				QDEC_Z0	I	Qdec z input channel 0 pin

6	4	30	5	P10	I/O	General-purpose digital input and output pin
				SPI0_MOSI	I/O	Spi0 mosi pin
				TIMER0_EXT	I	Timer0 external input pin
				ADC_CH5	AI	Adc channel 5 pin
				PWM0_CH4	O	Pwm0 channel 4 output pin
				KS_O4	O	Keyscan output channel 4 pin
7	5	31	6	P11	I/O	General-purpose digital input and output pin
				SPI0_MISO	I/O	Spi0 miso pin
				CLKTRIM_EXT	I	CLKTRIM external clock measurement input pin
				ADC_CH4	AI	Adc channel 4 pin
				PWM0_CH5	O	Pwm0 channel 5 output pin
				KS_O5	O	Keyscan output channel 5 pin
				I2S_MCLK	O	I2s output sample clock
8	6	32	7	P16	I/O	General-purpose digital input and output pin
				UART1_CTS	I	Uart1 cts pin
				ANT_SW4	O	Antenna switch 4 pin
				TIMER0_OUT	O	Timer0 output pin
				PWM0_CH6	O	Pwm0 channel 6 output pin
				KS_I6	I	Keyscan input channel 6 pin
				QDEC_Y0	I	Qdec y input channel 0 pin
-	-	33	8	P17	I/O	General-purpose digital input and output pin
				UART1_RTS	O	Uart1 rts pin
				TIMER1_OUT	O	Timer1 output pin
				PWM0_CH7	O	Pwm0 channel 7 output pin
				KS_I7	I	Keyscan input channel 7 pin
				QDEC_Y1	I	Qdec y input channel 1 pin
-	7	34	9	P26	I/O	General-purpose digital input and output pin
				UART1_CTS	I	Uart1 cts pin
				UART0_TX	O	Uart0 tx pin
				SPI1_MISO	I/O	Spi1 miso pin
				KS_O14	O	Keyscan output channel 14 pin
				PWM1_CH2	O	Pwm1 channel 2 output pin
-	-	35	10	P45	I/O	General-purpose digital input and output pin

				PWM2_CH0	O	Pwm2 channel 0 output pin
				KS_O22	O	Keyscan output channel 22 pin
9	8	36	11	P46	I/O	General-purpose digital input and output pin
				SWD_CLK	I	Swd clock input pin
				UART1_RX	I	Uart1 rx pin
				I2C0_SCL	I/O	I2c0 scl pin
				SPI0_CLK	I/O	Spi0 clock pin
				ANT_SW5	O	Antenna switch 5 pin
				KS_O0	O	Keyscan output channel 0 pin
10	9	37	12	P47	I/O	General-purpose digital input and output pin
				SWD_DAT	I/O	Swd data input output pin
				UART1_TX	O	Uart1 tx pin
				I2C0_SDA	I/O	I2c0 sda pin
				SPI0_CS	I/O	Spi0 cs pin
				ANT_SW6	O	Antenna switch 6 pin
				KS_O1	O	Keyscan output channel 1 pin
11	10	-	13	P06	I/O	General-purpose digital input and output pin
				SPI1_CS	I/O	Spi1 cs pin
				UART1_TX	O	Uart1 tx pin
				ANT_SW3	O	Antenna switch 3 pin
				PWM1_CH2	O	Pwm1 channel 2 output pin
				KS_O12	O	Keyscan output channel 12 pin
				QDEC_Y0	I	Qdec y input channel 0 pin
				I2S_MCLK	O	I2s output sample clock
12	11	-	14	P07	I/O	General-purpose digital input and output pin
				SPI1_CLK	I/O	Spi1 clock pin
				UART1_RX	I	Uart1 rx pin
				TIMER0_EXT	I	Timer0 external input pin
				PWM1_CH3	O	Pwm1 channel 3 output pin
				KS_O13	O	Keyscan output channel 13 pin
				QDEC_Y1	I	Qdec y input channel 1 pin
				ANT_SW5	O	Antenna switch 5 pin
-	-	-	15	P53	I/O	General-purpose digital input and output pin

				PWM1_CH3	O	Pwm1 channel 3 output pin
				KS_O3	O	Keyscan output channel 3 pin
				QDEC_Y_IDX	I	Qdec y_idx input pin
-	-	38	16	P54	I/O	General-purpose digital input and output pin
				PWM2_CH2	O	Pwm2 channel 2 output pin
				KS_O23	O	Keyscan output channel 23 pin
				QDEC_Z_IDX	I	Qdec z_idx input pin
-	-	39	17	P55	I/O	General-purpose digital input and output pin
				PWM2_CH3	O	Pwm2 channel 3 output pin
				KS_O4	O	Keyscan output channel 4 pin
				QDEC_X0	I	Qdec x input channel 0 pin
13	13	40	18	P56	I/O	General-purpose digital input and output pin
				PWM1_CH6	O	Pwm1 channel 6 output pin
				UART0_CTS	I	Uart0 cts pin
				UART1_TX	O	Uart1 tx pin
				QDEC_X0	I	Qdec x input channel 0 pin
				KS_O11	O	Keyscan output channel 11 pin
-	-	41	19	P57	I/O	General-purpose digital input and output pin
				PWM2_CH5	O	Pwm2 channel 5 output pin
				KS_O5	O	Keyscan output channel 5 pin
				QDEC_X1	I	Qdec x input channel 1 pin
-	-	42	20	P33	I/O	General-purpose digital input and output pin
				SPI0_CLK	I/O	Spi0 clock pin
				UART0_RTS	O	Uart0 rts pin
				PWM0_CH3	O	Pwm0 channel 3 output pin
				KS_O17	O	Keyscan output channel 17 pin
-	-	43	21	P32	I/O	General-purpose digital input and output pin
				SPI0_CS	I/O	Spi0 cs pin
				PWM0_CH2	O	Pwm0 channel 2 output pin
				KS_O16	O	Keyscan output channel 16 pin
-	-	44	22	P34	I/O	General-purpose digital input and output pin
				PWM2_CH4	O	Pwm2 channel 4 output pin
				KS_O18	O	Keyscan output channel 18 pin

				TIMER1_EXT	I	Timer1 external input pin
				ANT_SW2	O	Antenna switch 2 pin
-	-	45	23	P35	I/O	General-purpose digital input and output pin
				PWM2_CH5	O	Pwm2 channel 5 output pin
				KS_O19	O	Keyscan output channel 19 pin
				UART0_CTS	I	Uart0 cts pin
				ANT_SW3	O	Antenna switch 3 pin
-	-	46	24	P36	I/O	General-purpose digital input and output pin
				PWM2_CH6	O	Pwm2 channel 6 output pin
				KS_O20	O	Keyscan output channel 20 pin
				CLKTRIM_EXT	I	CLKTRIM external clock measurement input pin
				ANT_SW5	O	Antenna switch 5 pin
-	-	47	25	P37	I/O	General-purpose digital input and output pin
				PWM2_CH7	O	Pwm2 channel 7 output pin
				KS_O21	O	Keyscan output channel 21 pin
				KS_I2	I	Keyscan input channel 2 pin
				ANT_SW6	O	Antenna switch 6 pin
-	-	-	26	P51	I/O	General-purpose digital input and output pin
				PWM1_CH7	O	Pwm1 channel 7 output pin
				KS_O1	O	Keyscan output channel 1 pin
				QDEC_X_IDX	I	Qdec x_idx input pin
-	-	-	27	P50	I/O	General-purpose digital input and output pin
				PWM2_CH1	O	Pwm2 channel 1 output pin
				KS_O0	O	Keyscan output channel 0 pin
-	-	48	28	P22	I/O	General-purpose digital input and output pin
				QDEC_X_IDX	I	Qdec x_idx input pin
				PWM1_CH4	O	Pwm1 channel 4 output pin
				I2S_S_CLK	I	I2s slave data input pin
				SPI1_MISO	I/O	Spi1 miso pin
				KS_I2	I	Keyscan input channel 2 pin
				I2S_M_CLK	O	I2s master clock output pin
-	-	1	29	P23	I/O	General-purpose digital input and output pin
				QDEC_Y_IDX	I	Qdec y_idx input pin

				PWM1_CH5	O	Pwm1 channel 5 output pin
				I2S_S_WS	I	I2s slave chip select input pin
				SPI1_MOSI	I/O	Spi1 mosi pin
				KS_I3	I	Keyscan input channel 3 pin
				I2S_M_WS	O	I2s master chip select output pin
14	14	-	30	P04	I/O	General-purpose digital input and output pin
				I2S_S_SDI	I	I2s slave data input pin
				I2S_M_SDI	I	I2s master data input pin
				TIMER2_OUT	O	Timer2 output pin
				PWM1_CH0	O	Pwm1 channel 0 output pin
				KS_O10	O	Keyscan output channel 10 pin
				QDEC_X0	I	Qdec x input channel 0 pin
15	15	-	31	P05	I/O	General-purpose digital input and output pin
				I2S_S_SDO	O	I2s slave data output pin
				I2S_M_SDO	O	I2s master data output pin
				ANT_SW2	O	Antenna switch 2 pin
				PWM1_CH1	O	Pwm1 channel 1 output pin
				KS_O11	O	Keyscan output channel 11 pin
				QDEC_X1	I	Qdec x input channel 1 pin
				ADC_TRG	I	Adc external trg input pin
16	16	2	32	DVDD	P	Hldo output pin, typical value 1.2V
-	-	3	33	VIPIO2	P	Special io power supply pin（P40~P44）
-	-	4	34	P44	I/O	General-purpose digital input and output pin
				UART0_TX	O	Uart0 tx pin
				I2S_S_WS	I	I2s slave chip select input pin
				PWM2_CH4	O	Pwm2 channel 4 output pin
				I2S_M_WS	O	I2s master chip select input pin
-	-	5	35	P43	I/O	General-purpose digital input and output pin
				SPI0_MOSI	I/O	Spi0 mosi pin
				UART0_RX	I	Uart0 rx pin
				PWM2_CH3	O	Pwm2 channel 3 output pin
				I2S_MCLK	O	I2s output sample clock
				KS_O15	O	Keyscan output channel 15 pin

-	-	6	36	P42	I/O	General-purpose digital input and output pin
				SPI0_MISO	I/O	Spi0 miso pin
				I2S_S_SDO	O	I2s slave clock output pin
				PWM2_CH2	O	Pwm2 channel 2 output pin
				I2S_M_SDO	O	I2s master data output pin
-	-	7	37	P41	I/O	General-purpose digital input and output pin
				SPI0_CS	I/O	Spi0 cs pin
				I2S_S_SDI	I	I2s slave data input pin
				PWM2_CH1	O	Pwm2 channel 1 output pin
				I2S_M_SDI	I	I2s master data input pin
				I2C0_SCL	I/O	I2c0 scl pin
-	-	8	38	P40	I/O	General-purpose digital input and output pin
				SPI0_CLK	I/O	Spi0 clock pin
				I2C0_SDA	I/O	I2c0 sda pin
				I2S_S_CLK	I	I2s slave clock input pin
				I2S_M_CLK	O	I2s master clock output pin
				PWM2_CH0	O	Pwm2 channel 0 output pin
				KS_O2	O	Keyscan output channel 2 pin
-	-	-	39	P25	I/O	General-purpose digital input and output pin
				UART1_RX	I	Uart1 rx pin
				SPI1_CS	I/O	Spi1 cs pin
				ANT_SW1	O	Antenna switch 1 pin
				QDEC_Z_IDX	I	Qdec z_idx input pin
				KS_O9	O	Keyscan output channel 9 pin
				PWM1_CH1	O	Pwm1 channel 1 output pin
17	17	-	40	P24	I/O	General-purpose digital input and output pin
				UART1_TX	O	Uart1 tx pin
				SPI1_CLK	I/O	Spi1 clock pin
				ANT_SW0	O	Antenna switch 0 pin
				PWM1_CH0	O	Pwm1 channel 0 output pin
				KS_O8	O	Keyscan output channel 8 pin
				QDEC_Z0	I	Qdec z input channel 0 pin
18	18	9	41	P31	I/O	General-purpose digital input and output pin

				UART0_RX	I	Uart0 rx pin
				PWM1_CH7	O	Pwm1 channel 7 output pin
				SPI0_MISO	I/O	Spi0 miso pin
				ADC_CH0	AI	Adc input channel 0 pin
				KS_I5	I	Keyscan input channel 5 pin
19	19	10	42	P30	I/O	General-purpose digital input and output pin
				UART0_TX	O	Uart0 tx pin
				PWM1_CH6	O	Pwm1 channel 6 output pin
				SPI0_MOSI	I/O	Spi0 mosi pin
				ADC_CH1	AI	Adc input channel 1 pin
				KS_I4	I	Keyscan input channel 4 pin
-	-	-	43	P27	I/O	General-purpose digital input and output pin
				UART1_RTS	O	Uart1 rts pin
				UART0_RX	I	Uart0 rx pin
				SPI1_MOSI	I/O	Spi1 mosi pin
				ADC_CH2	AI	Adc input channel 2 pin
				KS_O15	O	Keyscan output channel 15 pin
				QDEC_Z1	I	Qdec z input channel 1 pin
20	20	11	44	P03	I/O	General-purpose digital input and output pin
				UART0_RTS	O	Uart0 rts pin
				ANT_SW1	O	Antenna switch 1 pin
				SPI0_CLK	I/O	Spi0 clock pin
				USB_DP	AI/AO	Usb dp pin
				PWM0_CH3	O	Pwm0 channel 3 output pin
				KS_I1	I	Keyscan input channel 1 pin
21	21	12	45	P02	I/O	General-purpose digital input and output pin
				UART0_CTS	I	Uart0 cts pin
				ANT_SW0	O	Antenna switch 0 pin
				SPI0_CS	I/O	Spi0 cs pin
				USB_DM	AI/AO	Usb dm pin
				PWM0_CH2	O	Pwm0 channel 2 output pin
				KS_I0	I	Keyscan input channel 0 pin
22	22	-	46	VOUT2_BK	P	DCDC-2 voltage output pin, power supply to internal Flash

23	23	13	47	VOUT1_BK	P	DCDC-1 voltage output pin, can be directly connected to VCC_RF pin
24	24	14	48	VSW1	P	DCDC internal power switch (switching frequency is about 650KHz), an external inductor is required when using
25	25	15	49	VSS_BK	P	Common ground terminal of DCDC power supply, independent power ground
26	26	16	50	VBAT_BK	P	(The power input pin of the chip, only in the QFN package) The power input pin of the DCDC provides power for the internal DCDC
-	-	17	51	P52	I/O	General-purpose digital input and output pin
				ADC_TRG	I	Adc external trg input pin
				SPI1_CS	I/O	Spi1 chip select pin
				ADC_CH3	AI	Adc input channel 3 pin
				KS_O2	O	Keyscan output channel 2 pin
				ANT_SW7	O	Antenna switch 7 pin
-	-	18	52	P15	I/O	General-purpose digital input and output pin
				UART1_RX	I	Uart1 rx pin
				ANT_SW7	O	Antenna switch 7 pin
				I2C0_SCL	I/O	I2c0 scl pin
				PWM0_CH5	O	Pwm0 channel 5 output pin
				KS_I5	I	Keyscan input channel 5 pin
				QDEC_X1	I	Qdec x input channel 1 pin
-	-	19	53	P14	I/O	General-purpose digital input and output pin
				UART1_TX	O	Uart1 tx pin
				I2C0_SDA	I/O	I2c0 sda pin
				ANT_SW6	O	Antenna switch 6 pin
				PWM0_CH4	O	Pwm0 channel 4 output pin
				KS_I4	I	Keyscan input channel 4 pin
				QDEC_X0	I	Qdec x input channel 0 pin
27	27	20	54	P13	I/O	General-purpose digital input and output pin
				I2C0_SDA	I/O	I2c0 sda pin
				I2S_S_WS	I	I2s slave chip select input pin
				I2S_M_WS	O	I2s master chip select output pin
				PWM0_CH7	O	Pwm0 channel 7 output pin
				ANT_SW4	O	Antenna switch 4 pin

				XL1	AO	External 32.768KHz clock source output
28	28	21	55	P12	I/O	General-purpose digital input and output pin
				I2C0_SCL	I/O	I2c0 clk pin
				I2S_S_CLK	I	I2s slave clock input pin
				I2S_M_CLK	O	I2s master clock output pin
				PWM0_CH6	O	Pwm0 channel 6 output pin
				XL0	AI	External 32.768KHz clock source input
-	-	-	56	VBAT	P	The power input pin of the chip
29	29	22	57	XC0	AI	External 32MHz clock source input
30	30	23	58	XC1	AO	External 32MHz clock source output
31	31	24	59	VCC_RF	P	RF power supply port, can be directly connected to VOUT1_BK pin
-	-	-	60	NC		
-	12	-	61	GND	P	Ground
32	32	25	62	ANT	AI/AO	RF antenna pin, an external antenna is required for use
-	-	-	63	GND	P	Ground
1	1	26	64	NRESET	I	Reset pin
33	33	49	-	E-PAD	P	Chip bottom pad, common ground (QFN package only)

5 Electrical specification

Maximum and minimum values

In the notes below each table, the data obtained through comprehensive evaluation, design simulation and/or process features are not tested on the production line; based on the comprehensive evaluation, the minimum and maximum values are after the sample test. Take the average value and add and subtract three times the standard distribution (average ± 3 Σ).

5.1 RF characteristics

Table 5-1 RF characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{OP}	Operating frequency		2400	-	2483	MHz
PLLres	PLL programming resolution		-	1	-	MHz
DR	Data rate		0.125	-	2	bps
$\Delta f_{BLE,2M}$	Frequency deviation @ BLE 2Mbps		450	500	550	kHz
$\Delta f_{BLE,1M}$	Frequency deviation @ BLE 1Mbps		225	250	275	kHz
$\Delta f_{297,2M}$	Frequency deviation @ 297mode 2Mbps		450	500	550	kHz
$\Delta f_{297,1M}$	Frequency deviation @ 297mode 1Mbps		225	250	275	kHz
$\Delta f_{N,2M}$	Frequency deviation @ N-mode 2Mbps		-	320	-	kHz
$\Delta f_{N,1M}$	Frequency deviation @ N-mode 1Mbps		-	170	-	kHz
$\Delta f_{BLE,2M}$	Channel spacing @ BLE 2Mbps		-	2	-	MHz
$\Delta f_{BLE,1M}$	Channel spacing @ BLE 1Mbps		-	2	-	MHz
$\Delta f_{297,2M}$	Channel spacing @ 297mode 2Mbps		-	2	-	MHz
$\Delta f_{297,1M}$	Channel spacing @ 297mode 1Mbps		-	1	-	MHz
$\Delta f_{N,2M}$	Channel spacing @ N-mode 2Mbps		-	2	-	MHz
$\Delta f_{N,1M}$	Channel spacing @ N-mode 1Mbps		-	1	-	MHz

Table 5-2 TX characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
P_{RFTX}	Output power		-	-	7	dBm
P_{RFC}	RF power control range		-	40	-	dB
P_{RFCR}	RF power accuracy		-	-	±3	dB
$P_{RF1M,1}$	1st Adjacent Channel Transmit Power @1Mbps		-	-32	-	dB
$P_{RF1M,2}$	2nd Adjacent Channel Transmit Power @1Mbps		-	-49	-	dB
$P_{RF1M,\geq 3}$	3rd Adjacent Channel Transmit Power @1Mbps		-	-54	-	dB

$P_{RF2M,2}$	1st Adjacent Channel Transmit Power @2Mbps		-	-21.5	-	dB
$P_{RF2M,4}$	2nd Adjacent Channel Transmit Power @2Mbps		-	-48	-	dB
$P_{RF2M,\geq 6M}$	3rd Adjacent Channel Transmit Power @2Mbps		-	-53	-	dB
P_{BW1M}	20dB bandwidth @1Mbps		-	1.3	-	MHz
P_{BW2M}	20dB bandwidth @2Mbps		-	2.3	-	MHz
$P_{SP,1}$	Spurious @≤1GHz		-	-	-63	dBm
$P_{SP,2}$	Spurious @≥1GHz		-	-	-43	dBm

Table 5-3 RX characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$P_{RX,MIX}$	Receive maximum input power		-	0	-	dBm
$P_{SENS,BLE,1M}$	Sensitivity, 1Mbps BLE		-	-96	-	dBm
$P_{SENS,BLE,2M}$	Sensitivity, 2Mbps BLE		-	-93	-	dBm
$P_{SENS,BLE,125K}$	Sensitivity, 125Kbps BLE		-	-99	-	dBm
$P_{SENS,BLE,500K}$	Sensitivity, 500Kbps BLE		-	-99	-	dBm
$P_{SENS,297,1M}$	Sensitivity, 1Mbps 297mode		-	-95	-	dBm
$P_{SENS,297,2M}$	Sensitivity, 2Mbps 297mode		-	-92	-	dBm
$P_{SENS,N,1M}$	Sensitivity, 1Mbps N-mode		-	-95	-	dBm
$P_{SENS,N,2M}$	Sensitivity, 2Mbps N-mode		-	-92	-	dBm
$C/I_{CO,1M}$	Co-Channel interference@1Mbps		-	21	-	dB
$C/I_{1M,1M}$	Adjacent (1 MHz) interference@1Mbps		-	15	-	dB
$C/I_{2M,1M}$	Adjacent (2 MHz) interference @1Mbps		-	-17	-	dB
$C/I_{\geq 3M,1M}$	Adjacent (≥3 MHz) interference @1Mbps		-	-27	-	dB
$C/I_{Image,1M}$	Image frequency interference@1Mbps		-	-9	-	dB
$C/I_{Image\pm 1M,1M}$	Adjacent (1 MHz) interference to in-band image frequency		-	-15	-	dB
$C/I_{\geq 6M,1M}$	Adjacent (≥6 MHz) interference @1Mbps		-	-27	-	dB
$C/I_{CO,2M}$	Co-Channel interference @2Mbps		-	21	-	dB
$C/I_{2M,2M}$	Adjacent (2 MHz) interference @2Mbps		-	15	-	dB
$C/I_{4M,2M}$	Adjacent (4 MHz) interference @2Mbps		-	-17	-	dB
$C/I_{\geq 6M,2M}$	Adjacent (≥6 MHz) interference @2Mbps		-	-27	-	dB
$C/I_{Image,2M}$	Image frequency interference @2Mbps		-	-9	-	dB
$C/I_{Image\pm 2M,2M}$	Adjacent (±2 MHz) interference to in-band image frequency		-	-15	-	dB

$C/I_{\geq 12M,2M}$	Adjacent (≥12 MHz) interference @2Mbps		-	-27	-	dB
$C/I_{CO,125K}$	Co-Channel interference @125Kbps		-	12	-	dB
$C/I_{1M,1M125K}$	Adjacent (1 MHz) interference @125Kbps		-	6	-	dB
$C/I_{2M,1M125K}$	Adjacent (2 MHz) interference @125Kbps		-	-26	-	dB
$C/I_{\geq 3M,1M125K}$	Adjacent (≥3MHz) interference @125Kbps		-	-36	-	dB
$C/I_{Image,1M125K}$	Image frequency interference @125Kbps		-	-18	-	dB
$C/I_{Image\pm 1M,125K}$	Adjacent (±1 MHz) interference to in-band image frequency @125Kbps		-	-24	-	dB
$C/I_{CO,500K}$	Co-Channel interference @500Kbps		-	17	-	dB
$C/I_{1M,500K}$	Adjacent (1 MHz) interference @500Kbps		-	11	-	dB
$C/I_{2M,500K}$	Adjacent (2 MHz) interference @500Kbps		-	-21	-	dB
$C/I_{\geq 3M,500K}$	Adjacent (≥3MHz) interference @500Kbps		-	-31	-	dB
$C/I_{Image,500K}$	Image frequency interference @500Kbps		-	-13	-	dB
$C/I_{Image\pm 1M,500K}$	Adjacent (±1 MHz) interference to in-band image frequency @500Kbps		-	-19	-	dB
$P_{IMD,5TH,1M}$	IMD performance 5 MHz offset @1Mbps		-	-30	-	dBm
$P_{IMD,5TH,2M}$	IMD performance 10 MHz offset @2Mbps		-	-31	-	dBm

Table 5-4 RSSI characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$RSSI_{RFC}$	RSSI indication range		-90	-	-15	dBm
$RSSI_{Auu}$	RSSI accuracy		-	±2	-	dB
$RSSI_{Res}$	RSSI resolution		-	0.25	-	dB
$RSSI_{Per}$	RSSI Sample period		-	15	-	us

Table 5-5 RF Timing characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$T_{OSC,EN}$	Crystal oscillator settling time		-	230	-	us
$T_{TX,EN}$	Time between TXEN task and READY event after channel FREQUENCY configured		-	TBD	-	us
$T_{RX,EN}$	Time between the RXEN task and READY event after channel FREQUENCY configured in default mode		-	TBD	-	us
$T_{TX,DISABLE}$	Time between DISABLE task and DISABLED event when the radio was in TX		-	TBD	-	us
$T_{RX,DISABLE}$	Time between DISABLE task and DISABLED event when the radio was in RX		-	TBD	-	us

T_{RX-TX}	The time taken to switch from RX to TX or TX to RX		-	150	-	us

Table 5-6 RF power characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$I_{TX,P6dBm,DCDC}$	TX only run current 6dBm @ DC-DC		-	15.2	-	mA
$I_{TX,P4dBm,DCDC}$	TX only run current 4dBm @DC-DC		-	9.6	-	mA
$I_{TX,P0dBm,DCDC}$	TX only run current 0dBm @DC-DC		-	6.1	-	mA
$I_{TX,P-4dBm,DCDC}$	TX only run current -4dBm @DC-DC		-	4.6	-	mA
$I_{TX,P-8dBm,DCDC}$	TX only run current -8dBm @DC-DC		-	3.8	-	mA
$I_{TX,P-12dBm,DCDC}$	TX only run current -12dBm @DC-DC		-	3.3	-	mA
$I_{TX,P-16dBm,DCDC}$	TX only run current -16dBm @DC-DC		-	3	-	mA
$I_{TX,P-20dBm,DCDC}$	TX only run current -20dBm @DC-DC		-	2.8	-	mA
$I_{TX,P-40dBm,DCDC}$	TX only run current -40dBm @DC-DC		-	2.2	-	mA
$I_{TX,P6dBm,LDO}$	TX only run current 6dBm @LDO		-	29.2	-	mA
$I_{TX,P4dBm,LDO}$	TX only run current 4dBm @LDO		-	16.6	-	mA
$I_{TX,P0dBm,LDO}$	TX only run current 0dBm @LDO		-	10.6	-	mA
$I_{TX,P-4dBm,LDO}$	TX only run current -4dBm @LDO		-	7.6	-	mA
$I_{TX,P-8dBm,LDO}$	TX only run current -8dBm @LDO		-	6.4	-	mA
$I_{TX,P-12dBm,LDO}$	TX only run current -12dBm @LDO		-	5.6	-	mA
$I_{TX,P-16dBm,LDO}$	TX only run current -16dBm @LDO		-	5.1	-	mA
$I_{TX,P-20dBm,LDO}$	TX only run current -20dBm @LDO		-	4.8	-	mA
$I_{TX,P-40dBm,LDO}$	TX only run current -40dBm @LDO		-	3.7	-	mA
$I_{RX,1M,DCDC}$	RX 1Mbps current @DC-DC		-	5.6	-	mA
$I_{RX,2M,DCDC}$	RX 2Mbps current @DC-DC		-	5.9	-	mA
$I_{RX,1M,LDO}$	RX 1Mbps current @LDO		-	9.6	-	mA
$I_{RX,2M,LDO}$	RX 2Mbps current @LDO		-	10.5	-	mA

Test conditions and methods.

1. Transceiver power consumption tested in 1M mode using BLE ADV broadcast mode
2. 2M mode is used is the power consumption when BLE connection
3. The power consumption tested is the RF peak power
4. The test method uses the total power consumption minus the power consumption of the MCU when the RF is not operating to calculate the final power consumption
5. The sample software tested is based on peripheral_hr

5.2 GPIO characteristics

Table 5-7 GPIO characteristics (single IO)

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{IH}	Input high voltage	TA=25°C	0.7*VDD	-	VDD	V
V_{IL}	Input low voltage	TA=25°C	VSS	-	0.2*VDD	V
V_{HYS}	Input hysteresis voltage, $V_{hys}=V_{IH}-V_{IL}$	TA=25°C	-	-	0.3*VDD	V
C_{Iana}	Analog input capacitors	Load capacitance =20pF, TA=25°	-	300	-	fF
I_{Lkg}	Leakage current, open-drain mode or input mode	VDD ≤ VIN ≤ 3.7V	-	-	2.5	uA
R_{PU}	Pull-up resistor	Vin =VSS, VDD =3.3V	48	50	52	kΩ
R_{PD}	Pull-down resistor	Vin =VSS, VDD =3.3V	98	100	102	kΩ
V_I	Input voltage	TA=25°C	VSS	-	VDD	V
$V_{I,P40-P44}$	Input voltage	TA=25°C	VSS	-	VIPIO2	V
V_O	Output voltage	TA=25°C	VSS	-	VDD	V
$V_{O,P40-P44}$	Output voltage	TA=25°C	VSS	-	VIPIO2	V
I_{OH}	Source current (Push-pull output)	Vin =VDD-0.5V	4.2	8	8.5	mA
	Source current (Quasi-bidirectional, high)		9	10	11	mA
I_{Sink}	Sink current (Push-pull output)	Vin =VSS+0.5V, TA=25°C	12	16	25	mA
I_{IO}*	Maximum sum of sink currents for all pins	VDD=3.3V, TA=25°C	-	-	108	mA
	Maximum sum of source currents for all pins		-	-	85	
f_{Port_CLK}	IO output frequency	Load capacitance =20pF	-	-	64	MHz

*Note: Current consumption must be correctly distributed across all I/O pins.

Table 5-8 Combined test

Description	Conditions	Status	Remark
IO default state after power on	VDD=3.3V ,TA=25°C	P46, P47 pull-up input state, other GPIOs are high resistance state	
IO status in deepsleep mode	VDD=3.3V ,TA=25°C	Under M0 except P56, P46, P47 (available), the rest are high resistance state, IO can be held	
IO status at reset	VDD=3.3V ,TA=25°C	P46, P47 pull-up input state, other GPIOs are high resistance state	

Table 5-9 nRESET Input Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{ILR}	Negative threshold voltage, nRESET	VDD=1.8V-3.3V ,TA=25°C	-	-	0.22*VDD	V
V_{IHR}	Positive threshold voltage, nRESET	VDD=1.8V-3.3V ,TA=25°C	0.48*VDD	-	-	V
V_{hys_rst}	Schmitt Trigger Voltage Hysteresis	VDD=1.8V-3.3V ,TA=25°C	-	-	0.26*VDD	V
R_{RST}	nRESET pin internal pull-up resistor	VDD=3.3V ,TA=25°C	4.6	4.8	5	kΩ
$t_{FR.\ 0.3pF}$	nRESET pin input filter pulse time	VDD=3.3V ,TA=25°C	-	20	-	ns

5.3 Reset characteristics

Table 5-10 Reset characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{BOD}	Brown-out detection voltage threshold	BODSEL<2:0> = 000(rising edge), dVDD/dt≤3V/s	-	2.19	-	V
		BODSEL<2:0> = 000(falling edge), dVDD/dt≤3V/s	-	2.08	-	
		BODSEL<2:0> = 001(rising edge), dVDD/dt≤3V/s	-	2.4	-	
		BODSEL<2:0> = 001(falling edge), dVDD/dt≤3V/s	-	2.29	-	
		BODSEL<2:0> = 010(rising edge), dVDD/dt≤3V/s	-	2.65	-	
		BODSEL<2:0> = 010(falling edge), dVDD/dt≤3V/s	-	2.53	-	
		BODSEL<2:0> = 011(rising edge), dVDD/dt≤3V/s	-	2.85	-	
		BODSEL<2:0> = 011(falling edge), dVDD/dt≤3V/s	-	2.72	-	
		BODSEL<2:0> =100(rising edge), dVDD/dt≤3V/s	-	3.09	-	
		BODSEL<2:0> = 100(falling edge), dVDD/dt≤3V/s	-	2.95	-	
		BODSEL;<2:0> = 101(rising edge), dVDD/dt≤3V/s	-	3.33	-	
		BODSEL<2:0> = 101(falling edge), dVDD/dt≤3V/s	-	3.17	-	
V_{BODhys}	BOD hysteresis voltage	dVDD/dt≤3V/s	100	-	160	mV
T_{BOD_RE1}	BOD response	dVDD/dt≤3V/s	2^4	2^4	2^15	1/SYS_CLK

	time，Normal mode					
I_{BOD}	BOD operating current	dVDD/dt≤3V/s	-	5	-	uA
V_{POR}	Power on reset voltage threshold	rising edge，dVDD/dt≤3V/s	-	1.7	-	V
		falling edge，dVDD/dt≤3V/s	-	1.7	-	V
T_{POR}	POR settling time	VBAT =3.3V	-	1.5	6.4	ms
V_{LVR}	LVR detection voltage threshold	falling edge，dVDD/dt≤3V/s	-	1.93	-	V
T_{LVR_RE}	LVR response time	TA=25°C，dVDD/dt≤3V/s	2^4	2^4	2^15	1/SYS_CLK
I_{LVR}	LVR operating current	TA=25°C，dVDD/dt≤3V/s	12.2	-	18.5	uA

5.4 Clock characteristics

Table 5-11 HXTAL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{HXTL}	High speed crystal oscillator (HXTAL) frequency	VDD=3.3V ,TA=25°C	-	32	-	MHz
$C_{LoadHXTL}$	Crystal load capacitance	VDD=3.3V ,TA=25°C	-	12	-	pF
I_{DDHXTL}	HXTAL oscillator operating current	VDD=3.3V ,TA=25°C	-	-	250	μA
t_{SUHXTL}	HXTAL oscillator startup time	VDD=3.3V ,TA=25°C, ESR=70Ω, C_{HXTL}= 13pF	-	200	-	μs
$t_{SUHXTL\ Quick}$	HXTAL oscillator Quick startup time	VDD=3.3V ,TA=25°C, ESR=70Ω, C_{HXTL}= 13pF	-	150	-	μs
ESR			-	50	80	Ω
$F_{TOLHXTL}$	Frequency tolerance for the crystal	VDD=3.3V ,TA=25°C	-20	-	20	ppm
PD_{HXTL}	Drive level	VDD=3.3V ,TA=25°C	-	-	100	μW

Table 5-12 LXTAL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{LXTL}	Low speed crystal oscillator (LXTAL) frequency	VDD=3.3V ,TA=25°C	-	32.768	-	kHz
I_{DDLXTL}	LXTAL oscillator operating current	VDD=3.3V ,TA=25°C	-	0.76	-	μA
t_{SULXTL}	LXTAL oscillator Normal startup time	VDD=3.3V ,TA=25°C	-	200	-	ms
$t_{SULXTL\ Quick}$	LXTAL oscillator Quick startup time	VDD=3.3V ,TA=25°C	-	2	-	ms
ESR_{LXTL}	Equivalent series resistance 6 pF < CL ≤ 9 pF	VDD=3.3V ,TA=25°C	-	100	-	kΩ
$C_{LoadLXTL}$	Crystal load capacitance	VDD=3.3V ,TA=25°C	-	12	-	pF
PD_{LXTL}	Drive level	VDD=3.3V ,TA=25°C	-	-	1	μW

Table 5-13 32MHz RCH characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{IRC32M}	Crystal frequency	VDD=3.3V ,TA=25°C	-	32	-	MHz
ACC_{IRC32M}	Frequency accuracy	VDD=3.3V, TA=-40°C ~+105°C	-	-	-	%
		VDD=3.3V, TA=-20°C ~ +85°C	-	-	-	%
		VDD=3.3V, TA=25°C	-2	1	2	%
D_{IRC32M}	IRC32M oscillator duty cycle	VDD=3.3V, fIRC32M=32MHz, TA=25°C	48	50	52	%
$I_{DDIRC32M}$	Operating current	VDD=3.3V, fIRC8M=32MHz, TA=25°C	200	390	480	μA
$t_{SUIRC32M}$	Startup time	VDD=3.3V, fIRC32M=32MHz, TA=25°C	-	5	-	μs
$d_{fIRC32M}$	25°C, The frequency drifts with the supply voltage	VDD=1.8V~3.7V, TA=25°C	-	0.5	-	%/V

Table 5-14 32kHz RCL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{IRC32k}	Crystal frequency	VDD=3.3V ,TA=25°C	-	32	-	kHz
ACC_{IRC32K}	Frequency accuracy	VDD=3.3V, TA=-40°C ~ +105°C (After calibration）	-	2000	-	ppm
D_{IRC32K}	IRC32K oscillator duty cycle	VDD=3.3V, f_{IRC32K}=32kHz, TA=25°C	7	-	16	%
$I_{DDIRC32K}$	Operating current	VDD=3.3V, f_{IRC8K}=32kHz, TA=25°C	-	700	-	nA
$t_{SUIRC32K}$	Startup time	VDD=3.3V, f_{IRC32K}=32kHz, TA=25°C	-	-	200	μs
df_{IRC32K}	25°C, The frequency drifts with the supply voltage	VDD=1.8V~3.7V, TA=25°C	-	5.5	-	%/V

Table 5-15 DPLL characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{PLLIN}	PLL input clock frequency	VDD=3.3V, TA=25°C	-	32	-	MHz
f_{PLL}	PLL output clock frequency	VDD=3.3V, TA=25°C	48	48	64*	MHz
I_{PLL}	Operating current	VDD=3.3V, TA=25°C	-	330	-	μA

Note: The 64MHz clock frequency requires special support.

5.5 ADC characteristics

Table 5-16 Power supply and input range conditions

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$V_{Ax(VBG\ adc)}$	Analog input voltage range, VBG（1.2V）	VDD=3.3V, TA=25°C	0	-	VBG_{ADC}	V
$V_{Ax(VDD)}$	Analog input voltage range, VDD	VDD=3.3V, TA=25°C	0	-	VDD	V
I_{ADC}	ADC supply current	VDD=3.3V, TA=25°C Fadc=16MHz	-	0.5	-	mA
C_{sample}	Internal sample and hold capacitors (PAD and PCB capacitors not included)		-	12	-	pF
R_{ADC}	Sampling switch resistance	0V ≤ VAx ≤ VDD	-	300	-	Ω
R_{In}	External input impedance, continuous sampling	0V ≤ VAx ≤ VDD	0.86	-	4734.70	kΩ

Table 5-17 ADC built-in voltage reference

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VBG_{ADC}	Internal 1.2V Reference Voltage	VDD=3.3V, TA=25°C	1.1	1.2	1.3	V
T_{Coef}	Temperature factor	TA=-40°C~105°C; VDD=1.8V~3.7V	-	-1	-	mV/°C

Table 5-18 Time parameters

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
F_{ADC}	ADC clock frequency	VDD=3.3V, TA=25°C	4	16	32	MHz
T_S	Sample time	VDD=3.3V, TA=25°C	4	1539	8192	$1/F_{adc}$
T_{CONV}	Conversion time	VDD=3.3V, TA=25°C	32	1580	8298	$1/F_{adc}$

Table 5-19 Linearity parameter

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
INL	Integral linearity error	VDD=3.3V, TA=25°C	-	-	±3	LSB
DNL	Differential linearity error	VDD=3.3V, TA=25°C	-	-	±3	LSB

SNR	Signal to Noise Ratio	Fadc = 16MHz Input Clock 250kHz VDD=3.3V, TA=25°C	-	64.3	-	dB
THD	Total harmonic distortion		-	75	-	dB
SFDR	Spurious-free signal dynamic range		-	77.29	-	dB
ENOB	Effective number of bits		-	10.33	-	Bit

Table 5-20 Temperature Sensor

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
T_{range}	Range	VDD=3.3V	-40	25	125	℃
Avg_{Slope}	Average slope	VDD=3.3V	-1.46	-2	-2.55	CODE/℃

Table 5-21 RIN

ADC significant bit	F_{ADC}(MHz)	Ts(cycles)	Ts(us)	Rinmax(kΩ)
12	32	4	0.125	0.86
12	32	8	0.25	2.01
12	32	32	1	8.95
12	32	64	2	18.20
12	32	128	4	36.69
12	32	8192	256	2367.20
12	16	4	0.25	2.01
12	16	8	0.5	4.32
12	16	32	2	18.20
12	16	64	4	36.69
12	16	128	8	73.68
12	16	8192	512	4734.70

Note: The sampling condition is continuous sampling.

5.6 PMU characteristics

Table 5-22 PMU characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{HLDO}	HLDO output voltage range, external capacitor	VDD=3.3V, TA=25°C	1.1	1.2	1.3	V
VDD_{PSRR}	Power supply rejection ratio of VDD	VDD=3.3V, TA=25°C	-15	-	-	dB

5.7 General operating conditions

Table 5-23 General operating conditions

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VDD*	Operating voltage	TA=25°C	1.8	-	3.7	V
VIPIO2*	Operating voltage	TA=25°C	1.8	-	3.7	V
T_{ST}	Storage temperature	-	-65	-	150	℃
T_A	Ambient temperature	-	-40	-	125	℃
$T_{J\text{-}LQFP64}$	Junction temperature	LQFP64(7x7x1.4)	-32	-	133	℃
$T_{J\text{-}QFN32}$	Junction temperature	QFN32L(5x5x0.5-0.5)	-36	-	129	℃
$R_{\theta JA\text{-}LQFP64}$	Thermal resistance	LQFP64(7x7x1.4)	-	76	-	℃/W
$R_{\theta JA\text{-}QFN32}$	Thermal resistance	QFN32L(5x5x0.5-0.5)	-	41	-	℃/W

Note: DCDC-OFF

5.8 DCDC characteristics

Table 5-24 DCDC characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{IN_DCDC}	Input voltage range	VDD=3.3V, TA=25°C	2	-	3.7	V
V_{OUT_DCDC}	Output voltage range	VDD=3.3V, TA=25°C	-	1.5	1.8	V
T_{EN_DCDC}	Standup time	VDD=3.3V ,I_{LOAD}=10mA, TA=25°C	-	200	-	us
η	Efficiency	VDD=3.3V ,I_{LOAD}=10mA, TA=25°C, L_{DCR}=80mΩ	-	83	-	%
$VRPL_{DCDC}$	Ripple	VDD=3.3V, TA=25°C	-	50	-	mv
I_{OUT}	Drive peak current	VDD=3.3V, TA=25°C	-	-	150	mA
I_{AVG}	Drive average current	VDD=3.3V, TA=25°C	-	-	30	mA
L_{DCDC}	Effective inductance	VDD=3.3V, TA=25°C	-	2.2	-	μH
C_{OUT_DCDC}	Effective load capacitance	VDD=3.3V, TA=25°C	-	4.7	-	μF
F_{osc_DCDC}	Oscillation frequency	VDD=3.3V, TA=25°C	100	-	1000	kHz

5.9 ESD characteristics

Table 5-25 ESD characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VESDHBM[1]	ESD @ Human Body Mode	TA=25°C	-	±2.5（LQFP64） ±5（QFN48） ±4（QFN32）	-	kV

VESDCDM[2]	ESD @ Charge Device Mode	TA=25°C	-	±500	-	V
VESDMM[3]	ESD @ machine Mode	TA=25°C	-	±250（LQFP64） ±250（QFN48） ±300（QFN32）	-	V
$I_{latchup}$[4]	Latch up current	TA=25°C	-	±500	-	mA

Notes:

1. Determined by ANSI/ESDA/JEDEC JS-001 standard, Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) - Device Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 Electrostatic Discharge Sensitivity (ESD) Test Standard.
3. Determined according to JESD22-A115-C electrostatic discharge sensitivity (ESD) test standard.
4. Determined according to JEDEC EIA/JESD78 standard.

5.10 Absolute maximum ratings

Table 5-26 Absolute maximum ratings

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VDD - VSS	Supply voltages	TA=25°C	-0.3	-	3.7	V
VIN	I/O pin voltage	TA=25°C	VSS-0.3	-	VDD + 0.3	V
PVDD	Extreme power consumption	VDD=3.3V, TA=25°C DCDC power supply	-	-	250	mW

5.11 MCU current characteristics

Symbol	Parameter	Conditions		DCDC ON	DCDC OFF
				Typ(mA)	Typ(mA)
Run mode	All peripherals clockon, run while(1) in flash	System clock source: RCH	4M	0.786	1.1
			8M	1.35	1.93
			16M	2.1	3.05
			32M	3.61	5.43
		System clock source: XTH	4M	1.36	1.97
			8M	1.93	2.8
			16M	2.68	3.93
			32M	4.19	6.18
		System clock source: DPLL	16M	3.18	4.67
			24M	3.93	5.78
			32M	4.7	6.95
			48M	6.21	9.18
			64M	7.7	11.44

	All peripherals clockoff, run while(1) in flash	System clock source: RCH	4M	0.75	1.05
			8M	0.92	1.31
			16M	1.24	1.79
			32M	1.86	2.69
		System clock source: XTH	4M	1.05	1.5
			8M	1.22	1.75
			16M	1.57	2.26
			32M	2.23	3.25
		System clock source: DPLL	16M	1.86	2.7
			24M	2.2	3.21
			32M	2.57	3.76
			48M	3.25	4.77
			64M	3.97	5.84

Notes: Test conditions - DVDD=1.2V, VDD=3.3V, VBG=1.2V, TA=25°C

Symbol	Parameter	Conditions		Typ(μA)
standby m0	all sram lost	wake by 32k timer	RCL	1.14
			XTL	1.14
		wake by gpio p56		0.34
standby m1	all sram lost	wake by 32k timer	RCL	1.39
			XTL	1.39
		wake by gpio p56		0.59
	all sram retention	wake by 32k timer	RCL	4.62
			XTL	4.62
		wake by gpio p56		3.99
	sram0 32k on	wake by 32k timer	RCL	2.41
			XTL	2.41
		wake by gpio p56		1.7
	sram1 16k on	wake by 32k timer	RCL	1.98
			XTL	1.98
		wake by gpio p56		1.26
	sram2 8k on	wake by 32k timer	RCL	1.76
			XTL	1.76
		wake by gpio p56		1
	sram3 8k on	wake by 32k timer	RCL	1.76
			XTL	1.76
		wake by gpio p56		1
	LL sram retention	wake by 32k timer	RCL	2.2
			XTL	2.2
		wake by gpio p56		1.46
	Decrypt sram retention	wake by 32k timer	RCL	1.47
			XTL	1.47
		wake by gpio p56		0.73
Deepsleep	all sram lost	wake by 32k timer	RCL	1.36
		wake by external P56		0.59

	all sram retention	wake by 32k timer	RCL	8.19
		wake by external P56		7.62
		wake by gpio all		7.57
		wake by peripheral timer	RCL+TIMER	8.41
		wake by peripheral wdt	RCL+WDT	8.43
		wake by peripheral kscan	RCL+KSCAN	8.59
		wake by peripheral qdec	RCL+QDEC	8.45
	sram0 32k on	wake by 32k timer	RCL	9.18
		wake by external P56		8.83
	sram1 16k on	wake by 32k timer	RCL	8.78
		wake by external P56		8.34
	sram2/sram3 8k on	wake by 32k timer	RCL	8.53
		wake by external P56		8.07
	LL sram retention	wake by 32k timer	RCL	8.98
		wake by external P56		8.57
	Decrypt sram retention	wake by 32k timer	RCL	8.25
		wake by external P56		7.81

Notes: Test conditions - DVDD=1.2V, VDD=3.3V, VBG=1.2V, TA=25°C

6 Application Reference Diagram

LQFP64 application reference diagram

PAN1080LA5A / PAN1080LB5A / PAN1080LB5B

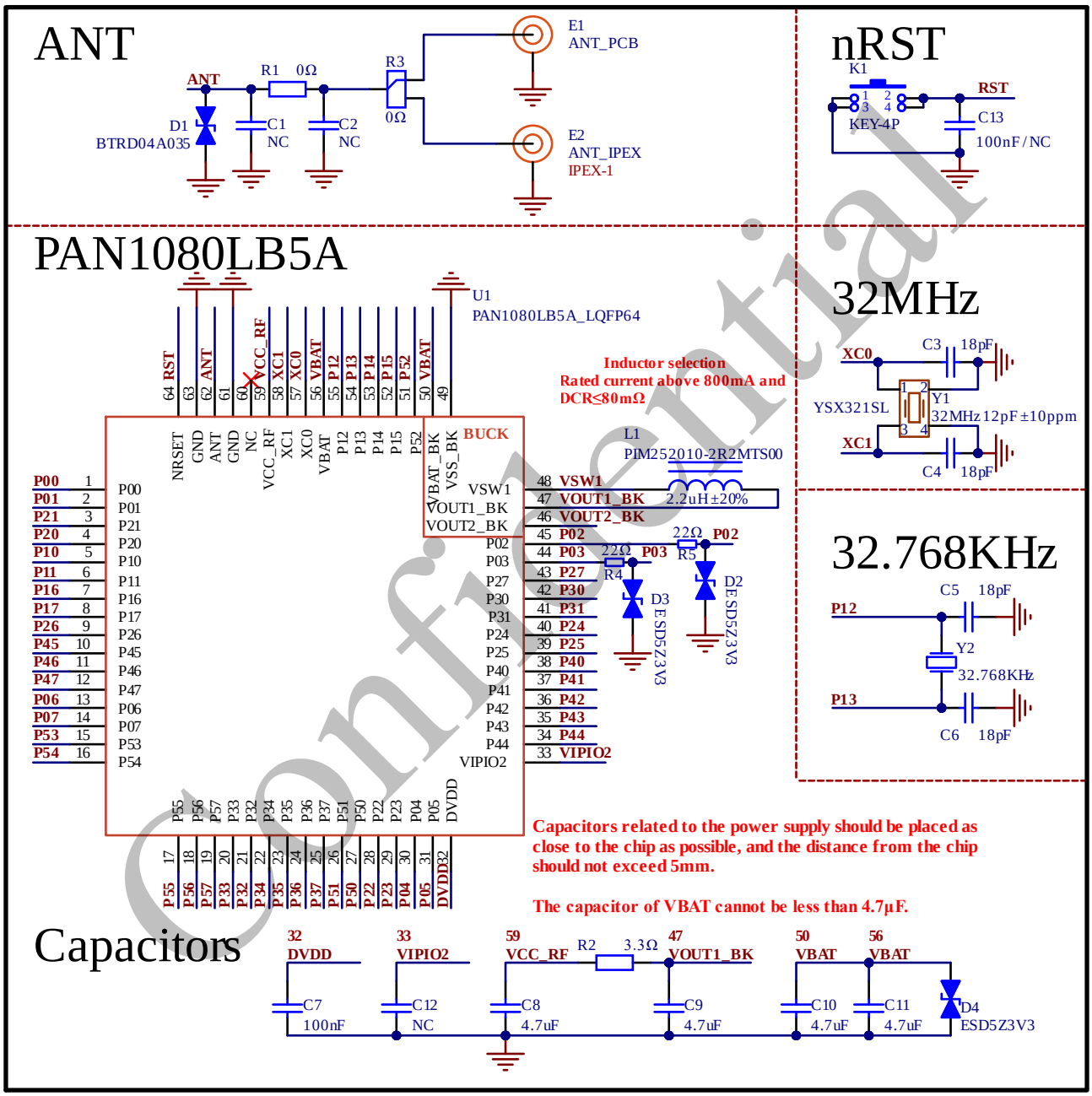


Figure 6-1 Application Schematic of the LQFP64

QFN48 application reference diagram

PAN1080UA3C

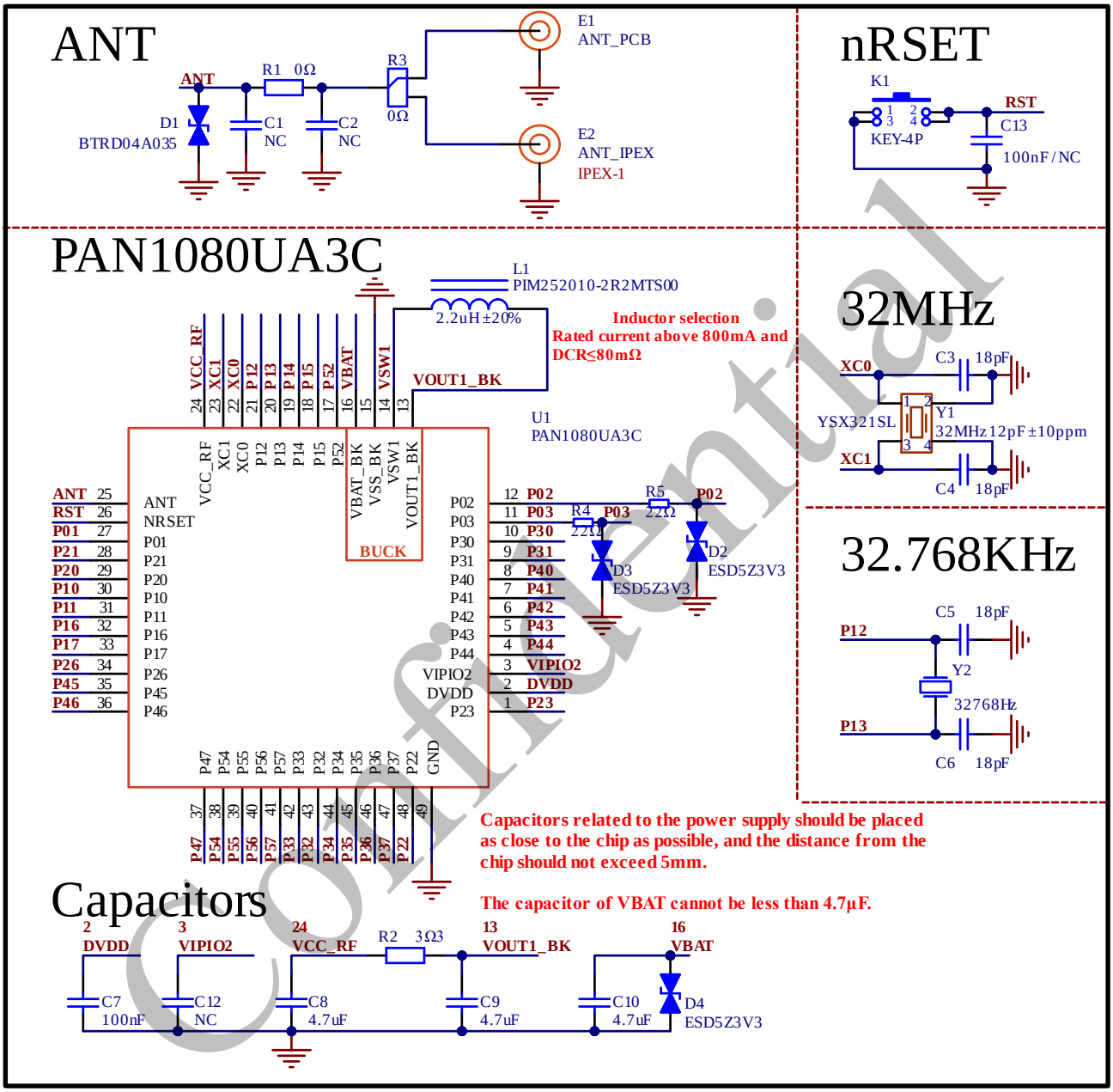


Figure 6-2 Application Schematic of the QFN48

QFN32(5×5) application reference diagram

PAN1080UB1A / PAN1081UB1A / PAN1082UA1C

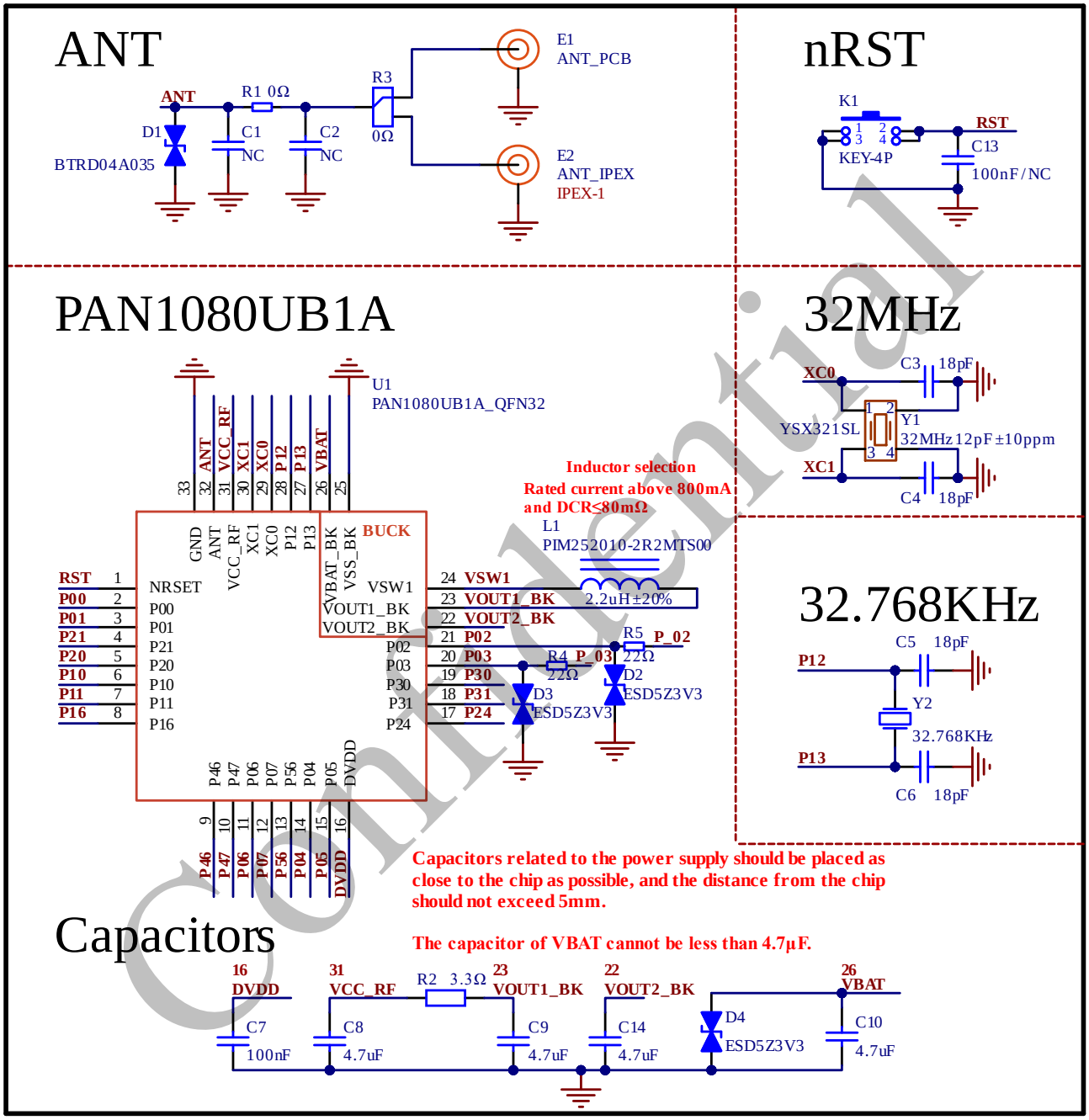


Figure 6-3 Application Schematic of the QFN32(5×5)

QFN32(4×4) application reference diagram

PAN1083UA1C

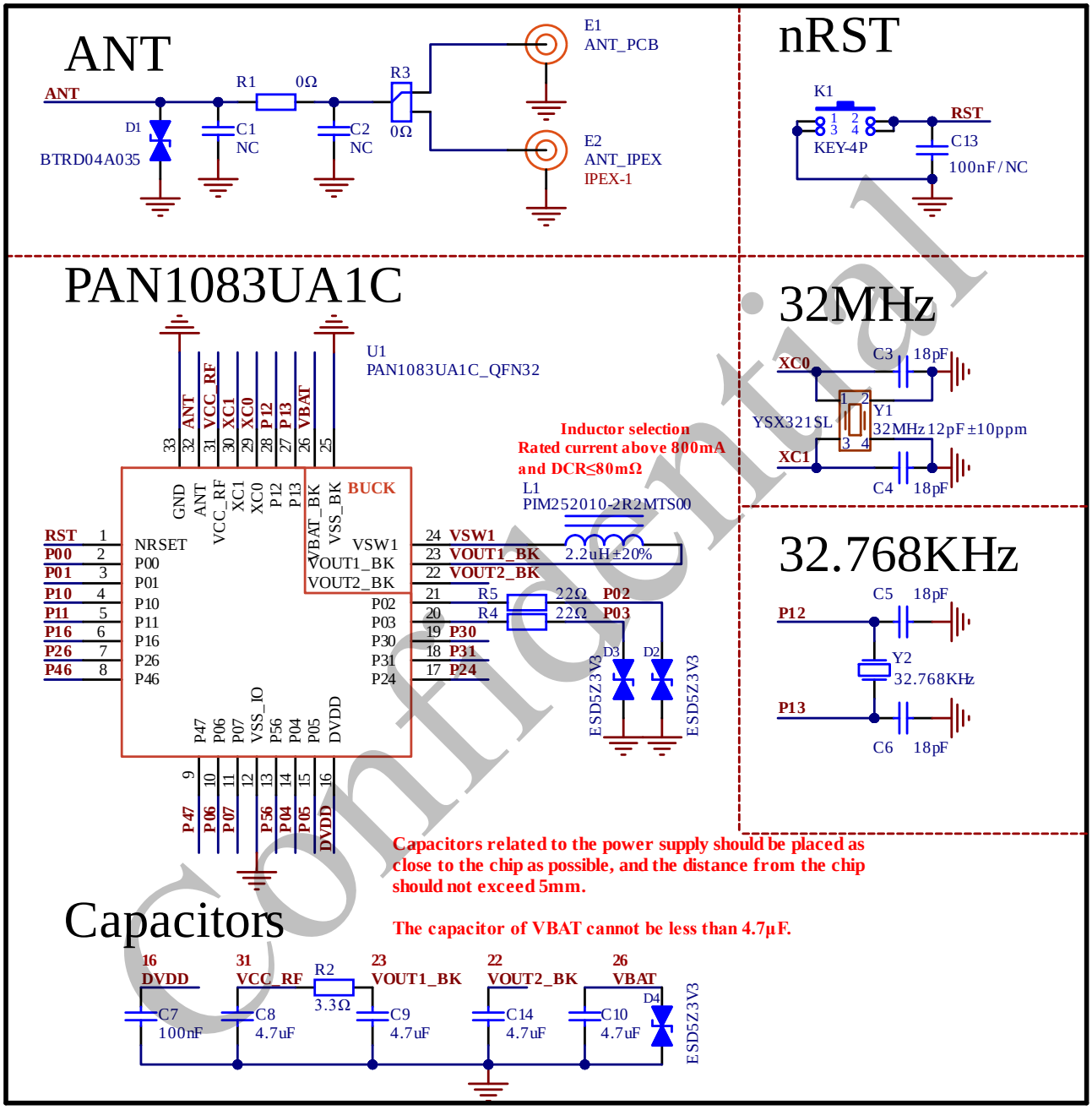


Figure 6-4 Application Schematic of the QFN32(4×4)

7 Package Dimensions

7.1 QFN32 package

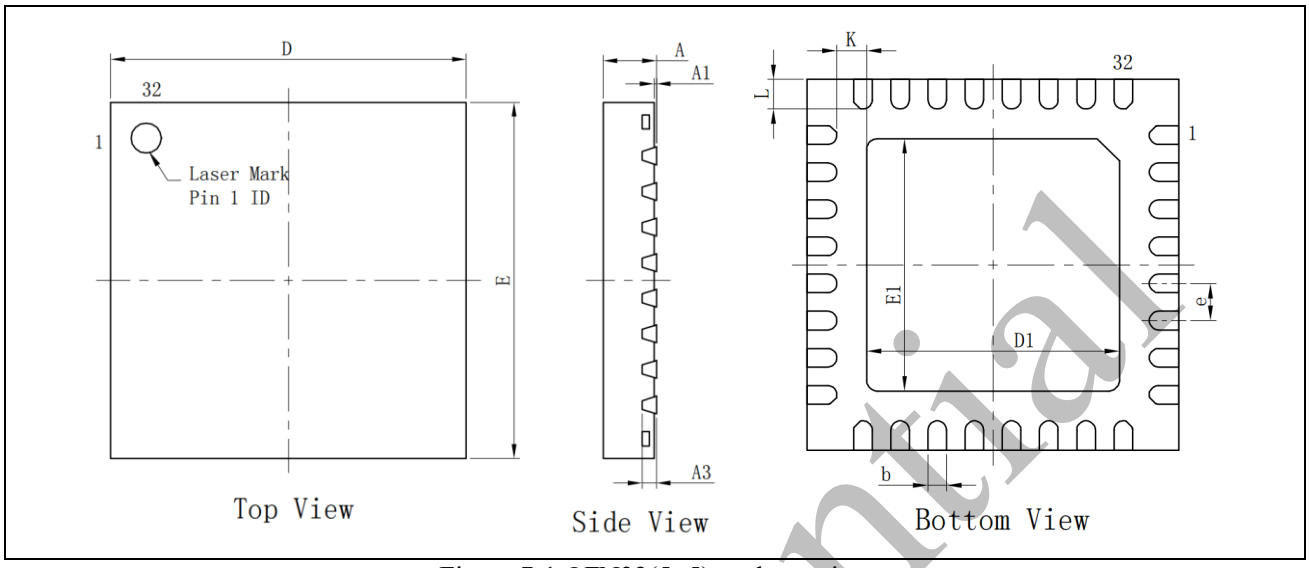


Figure 7-1 QFN32(5×5) package view

Table 7-1 QFN32(5×5) package dimension

SYMBOL	MIN（mm）	NOM（mm）	MAX（mm）
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D1	3.30	3.40	3.50
E1	3.30	3.40	3.50
e	0.50TYP		
K	0.20	-	-
L	0.32	0.40	0.48

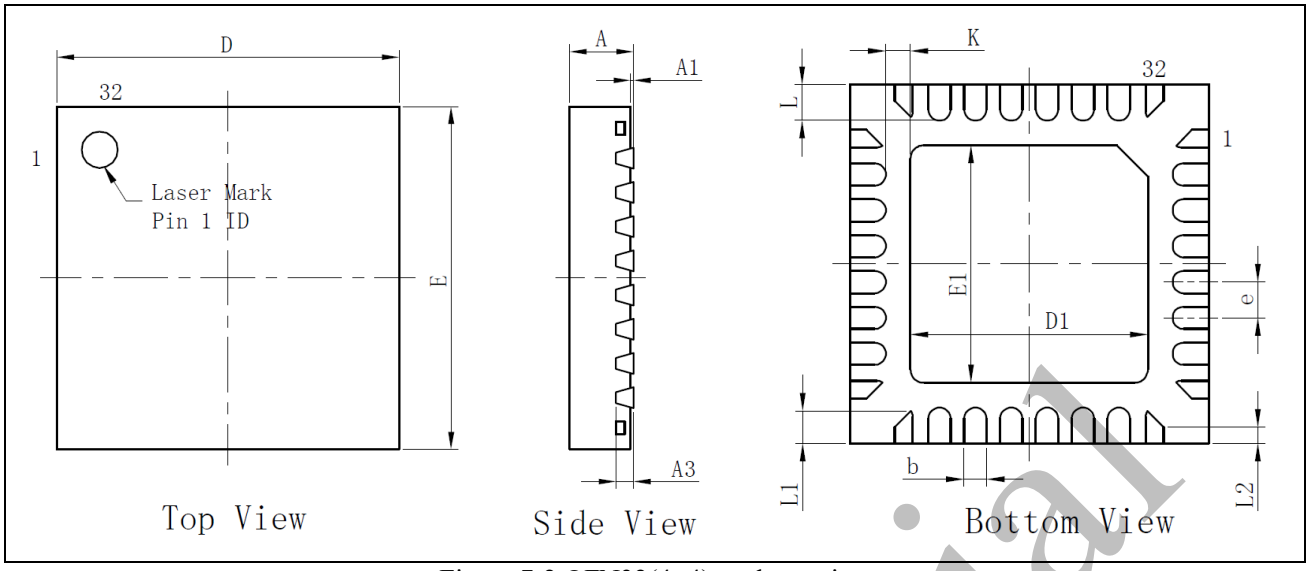


Figure 7-2 QFN32(4×4) package view

Table 7-2 QFN32(4×4) package dimension

SYMBOL	MIN（mm）	NOM（mm）	MAX（mm）
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.55	2.65	2.75
E1	2.55	2.65	2.75
e	0.40TYP		
K	0.20	-	-
L	0.30	0.40	0.50
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23

7.2 QFN48 package

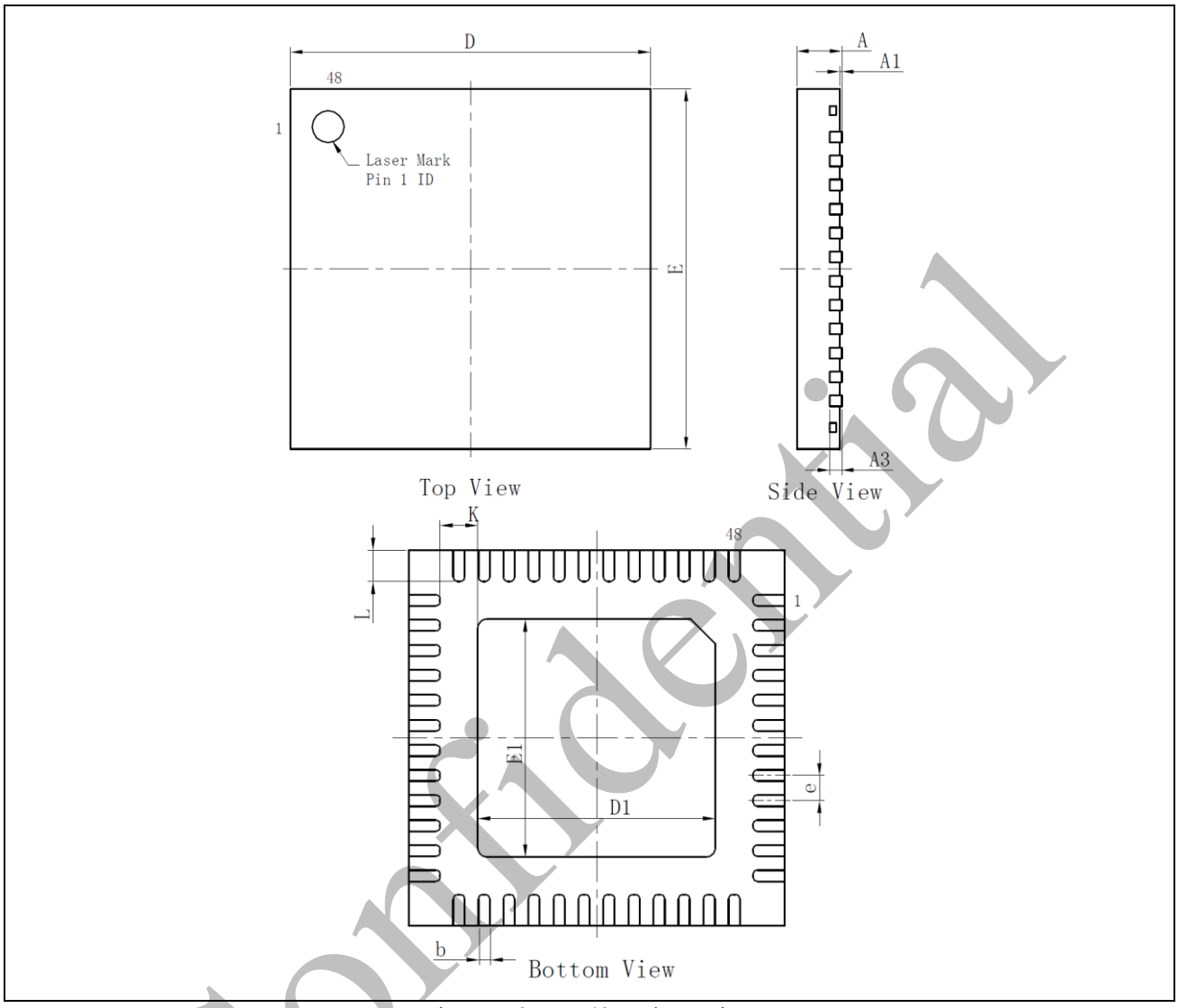


Figure 7-3 QFN48 package view

Table 7-3 QFN48 package dimension

SYMBOL	MIN（mm）	NOM（mm）	MAX（mm）
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.203REF		
b	0.13	0.18	0.23
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D1	3.70	3.80	3.90
E1	3.70	3.80	3.90
e	0.40TYP		
K	0.20	-	-
L	0.45	0.50	0.55

7.3 LQFP64 package

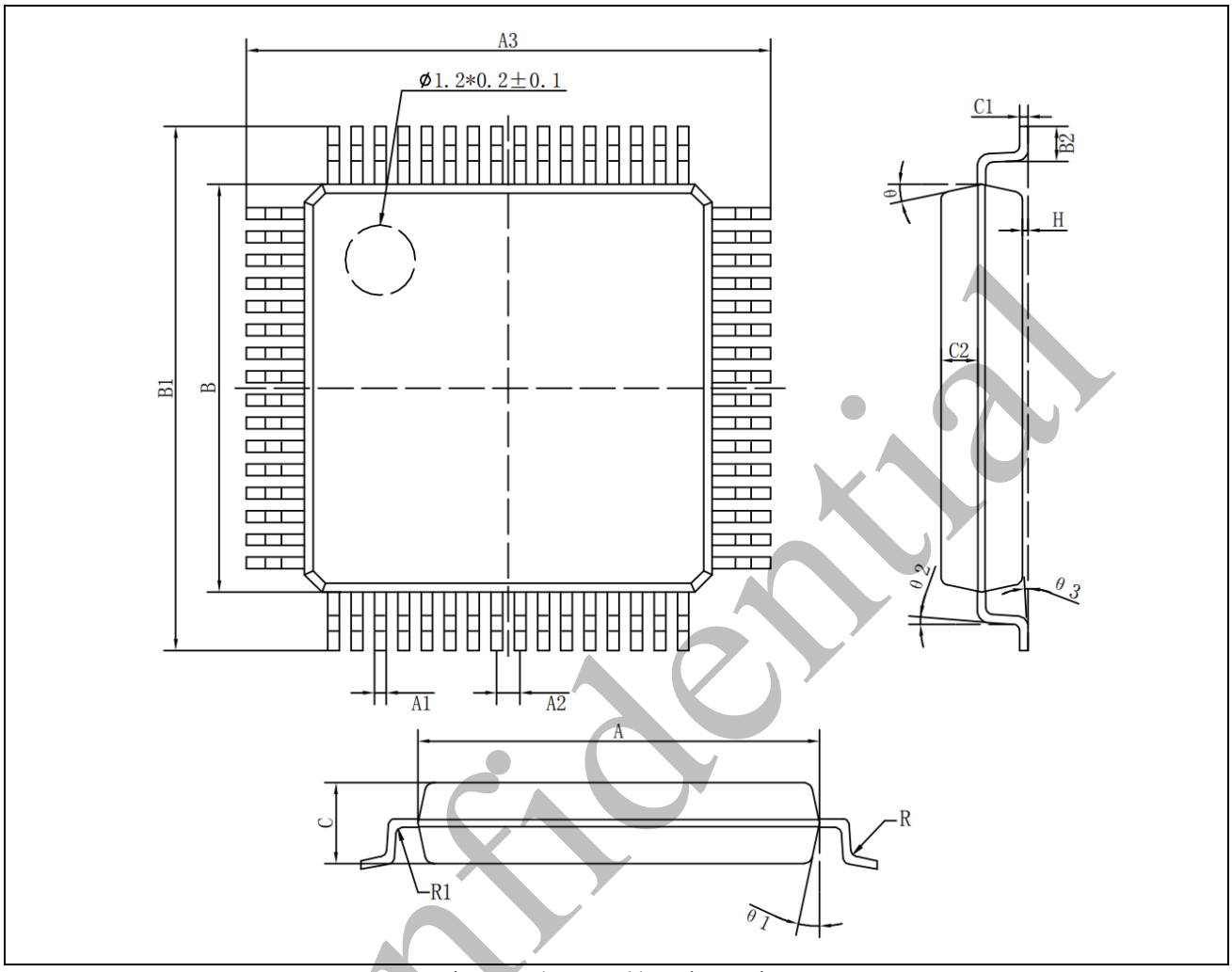


Figure 7-4 LQFP64 package view

Table 7-4 LQFP64 package dimension

SYMBOL	MIN（mm）	MAX（mm）
A	6.90	7.10
A1	0.18TYP	
A2	0.40TYP	
A3	8.80	9.20
B	6.90	7.10
B1	8.80	9.20
B2	0.50	0.80
C	1.30	1.50
C1	0.127	0.16
C2	0.636TYP	
H	0.05	0.15
θ	12°TYP4	
θ1	12°TYP4	
θ2	4°TYP4	

θ3	0°~ 5°
R	0.15TYP
R1	0.12TYP

Abbreviation

A	
APB	Advanced Peripheral Bus
ADC	Analog-to-Digital Converter
ALT	Alternate Function Select
ANAC	Analog Control
APROM	Application ROM
ATT	Attribute Protocol
B	
BAUDR	Baud Rate Select Register
BLDC	Brushless Direct Current Motor
Bluetooth LE	Bluetooth Low Energy
BOD	Brown-out Detector
BOM	Bill of Materials
C	
CFGx	Configuration Register for Channel x
ChEnReg	DMA Channel Enable Register
CMPDAT	Compare value
CPU	Central Processing Unit
CRC-32	Cyclic Redundancy Check
CTLx	Control Register for Channel x
CTRLR0	Control Register 0
CTRLR1	Control Register 1
D	
DARx	Destination Address Register for Channel x
Desiccant	A material for adsorbing moisture while remaining dry
DFBA	Data Flash Base Address Register
DLF	Divisor Latch Fraction Register
DLH	Divisor Latch High
DLL	Divisor Latch Low
DmaCfgReg	DMA Configuration Register
DMACR	DMA Control Register
DmaIdReg	DMA ID Register
DMARDLR	DMA Receive Data Level Register
DMASA	DMA Software Acknowledge
DMATDLR	DMA Transmit Data Level Register
DR	Data Register
DSTATARx	Destination Status Address Register for Channel x
DSTATx	Destination Status Register for Channel x
E	
ESD	Electro-Static discharge
F	
FCR	FIFO Control Register
FIFO	First Input First Output
FMC	Flash Memory Controller
Floor life	The longest time that the HiSilicon product is allowed to remain in the workshop (environ-ment <30 °C / 60% RH, before unpacking the moisture-proof packaging to reflow).
G	
GAP	Generic Access Profile
GATT	Generic Attribute Profile
GPIO	General-purpose I/O
H	
HCLK	Tstem Clock
HIC	Humidity Indicator Card
HID	Human Interface Device
HIRC	32MHz internal high speed oscillator
HTX	Halt TX
HXT	32MHz external high speed crystal oscillator
I	
I2C	Inter-Integrated Circuit
IAP	In-Application-Programming
ICE	In-Circuit-Emulator
ICP	In-Circuit Programming
ICR	Interrupt Clear Register
IDR	Identification Register
IER	Interrupt Enable Register
IIR	Interrupt Identity Register
IMR	Interrupt Mask Register
IRSR	Interrupt Raw Status Registers
ISB	Instruction Synchronization Barrier
ISP	In-System Programming
ISR	Interrupt Service Routine
L	
L2CAP	Logical Link Control and Adaptation Protocol
LCR	Line Control Register
LCR_EXT	Line Extended Control Register
LDO	Low dropout regulator
LDROM	Loader ROM
LIRC	32 kHz internal low speed RC oscillator
LNA	Low Noise Amplifier

LSB	Least significant bit
LSR	Line Status Register
LstDstReg	Last Destination Transaction Request Register
LstSrcReg	Last Source Transaction Request Register
LVR	Low Voltage Reset
LXT	32.768 kHz external low speed crystal oscillator
M	
MBB	Moisture Barrier Bag
MCR	Modem Control Register
MCU	Micro Control Unit
MDM	Mobile Device Management
MFP	Multiple Function Port
MISO	Master input slave output
MOSI	Master output slave input
MSB	Most Significant Bit
MSL	Moisture sensitivity level, this product is on level 3
MSR	Modem Status Register
MSTICR	Multi-Master Interrupt Clear Register
N	
NMI	Non Maskable Interrupt
NVIC	Nested Vectored Interrupt Controller
P	
PA	Power Amplifier
PLL	Phase Locked Loop
POR	Power-on Reset
PWM	Pulse Width Modulation
R	
RAR	Receive Address Register
RBR	Receive Buffe Register
ReqDstReg	Destination Software Transaction Request Register
ReqSrcReg	Source Software Transaction Request Register
RF	Radio frequency
RFL	Receive FIFO Level
RISR	Raw Interrupt Status Register
ROM	Read-Only Memory
RSSI	Received Signal Strength Indication
RTOS	Real Time Operating System
RXFLR	Receive FIFO Level Register
RXFTLR	Receive FIFO Threshold Level Register
RXOICR	Receive FIFO Overflow Interrupt Clear Register
RXUICR	Receive FIFO Underflow Interrupt Clear Register
S	
SARx	Source Address Register for Channel x Register
SCB	System Control Block Registers
SCB	System Control Block Registers
SCR	Scratchpad Register
SER	Slave Enable Register
SglReqDstReg	Single Destination Transaction Request Register
SglReqSrcReg	Single Source Transaction Request Register
Shelf Life	Normal storage time after moisture-proof packaging
SM	Security Manager
SoC	System on chip
SPI	Serial Peripheral Interface
SPROM	Security protection ROM
SR	Status Register
SRAM	Static random access memory
SSTATARx	Source Status Address Register for Channel x
SSTATx	Source Status Register for Channel x
Statusint	Combined Interrupt Status Register
SWD	Serial Wire Debug
SysTick	System Timer
T	
TAR	Transmit Address Register
TFL	Transmit FIFO Level
THR	Transmit Holding Register
THRE	Transmitter Holding Register Empty
TMR	Timer Controller
TXFLR	Transmit FIFO Level Register
TXFTLR	Transmit FIFO Threshold Level Register
TXOICR	Transmit FIFO Overflow Interrupt Clear Register
U	
UART	Universal Asynchronous Receiver/Transmitters
USR	UART Status Register
W	
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Revision History

Version	Date	Content
1.0	Jun.2021	Initial

USING THIS DOCUMENT

The information in this document is subject to change without notice. Every effort has been made in the preparation of this document to ensure the accuracy of the contents, but all statements, information, and recommendations in this document do not constitute a warranty of any kind, express or implied.

TRADEMARKS

Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

DISCLAIMER

All or part of the products, services and features described in this document may not be within the purchase scope or the usage scope. Unless otherwise specified in the contract, all statements, information, and recommendations in this document are provided “AS IS” without warranties, guarantees or representations of any kind, either express or implied.

Contact Us

Shanghai Panchip Microelectronics Co., Ltd.
The 302 Room of Building D, No. 666 Shengxia Road
Zhangjiang Hi-Tech Park, Shanghai
People's Republic of China

021-50802371

http://www.panchip.com