PANCHIP

PAN271x series

Datasheet

V1.4 Feb. 2026

Panchip Microelectronics Co., Ltd.

2.4GHz High-speed SoC Transceiver

General Description

PAN271x integrates 2.4GHz wireless SoC transceiver. The wireless transceiver circuit works in the 2.400-2.483GHz universal ISM frequency band. There is a 16KB OTP internal program memory and a built-in 3KB SRAM memory. In addition, PAN271x is equipped with a wealth of peripherals, including up to 19 GPIOs, 6-channel PWM, 1 25-bit timer, 1 32-bit SLPTMR, 1 I2C, 2 UARTs, 1 SPI, 1 ADC, WDT, etc.

Key Features

- **MCU**
  - 32-bit MCU core running up to 48 MHz
- **Memory**
  - Up to 16KB OTP supporting deep sleep mode
  - Up to 3KB SRAM
  - 2K bits EEPROM (PAN2713 only)
- **Low Power**
  - Active mode RX (whole chip): 10mA
  - Active mode TX at 0dBm (whole chip): 13mA
  - Standby mode0 (external interrupts): 0.82uA
  - Standby mode1 (external interrupts, SLPTMR, 3KB SRAM retention): 1.12uA
  - Deep sleep mode1 (external interrupts, SLPTMR, chip retention): 1.68uA
- **Clock**
  - 32M RC / 32.768kHz RC
  - 32M XTAL / 32.768kHz XTAL
  - DPLL(Two channels: 32M/48M)
- **RF**
  - Mode
    - 2.4G private protocol: 2Mbps / 1Mbps / 500kbps /250kbps / 125kbps, supporting hardware ACK
  - Output power: -55 to 11dBm
  - Receiver
    - -94dBm @ 1Mbps
    - -91dBm @ 2Mbps
    - -99dBm @ 250kbps
    - -98dBm @ 500kbps
    - -100dBm @ 125kbps
  - RSSI
    - Resolution: 0.25dB
    - Accuracy: ±2dB
    - Range: -90 to -15dBm
  - Single antenna supported
  - Safety regulations: ETSI / FCC
- **Peripheral**
  - Up to 19 GPIOs
  - 6-channel PWM
  - 1 25-bit timer
  - 1 32-bit SLPTMR
  - 1 I2C / 1 SPI
  - 2 UARTs
  - Up to 21-channel ADC (18 ext, bandgap, VDD/2, temp)
  - 1 WDT / 1 Keyscan
  - IO / BOD / POR / System reset
  - 1 Clock measurement
- **Power Management**
  - Integrated voltage regulator
  - Support USB 5V supply
  - Operating voltage (VBAT): 1.8 to 3.8V
  - Operating voltage (VUSB): 4.5 to 5.5V
- **Package:**
  - SSOP24 / SOP16 / SOP14 / MSOP10
- **Operating Condition**
  - Operating temperature: -40 to 85℃
  - Storage temperature: -60 to 150℃
  - ESD
    - HBM: ±2KV
    - MM: ±200V
    - CDM: ±2000V
    - Latch-up: ±100mA

Typical Applications

- Wireless remote control
- Smart home & security
- Wireless mouse & keyboard
- Wireless game controller
- Toys and wireless audio
- Active tag

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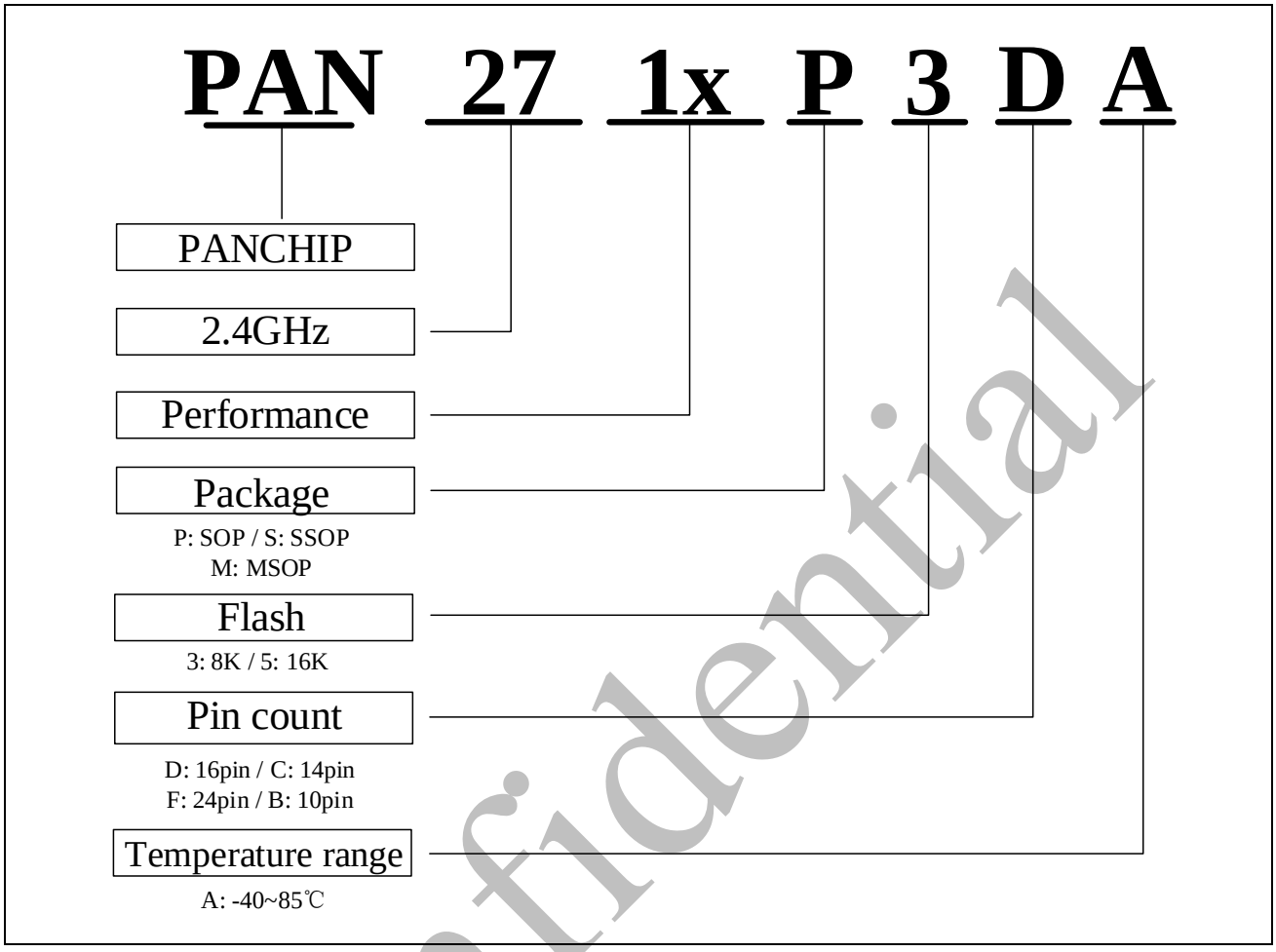
1 Naming Rule



2 Ordering Information

Part Number	Type	EEPROM	USB	Package	Pin Count	IO	OTP	SRAM	Temperature Range	Packing
PAN2710 S5FA	2.4GHz	×	○	SSOP	24	19	16KB	3KB(1)	-40 to 85℃	Tube
PAN2710 M5BA	2.4GHz	×	○	MSOP	10	4	16KB	3KB(1)	-40 to 85℃	Tape&Reel
PAN2711 P3DA	2.4GHz	×	×	SOP	16	11	8KB	2KB	-40 to 85℃	Tube
PAN2711 P3CA	2.4GHz	×	×	SOP	14	9	8KB	2KB	-40 to 85℃	Tube
PAN2712 P3DA(2)	2.4GHz	×	×	SOP	16	11	8KB	2KB	-40 to 85℃	Tube
PAN2713 M5BA	2.4GHz	○	○	MSOP	10	4	16KB	3KB(1)	-40 to 85℃	Tape&Reel

Before ordering, please contact the sales window for the latest mass production information.

(1)Share 1KB with USB.

(2)For details on the differences between PAN2711P3DA and PAN2712P3DA, please refer to Pin Information.

3 Block Diagram

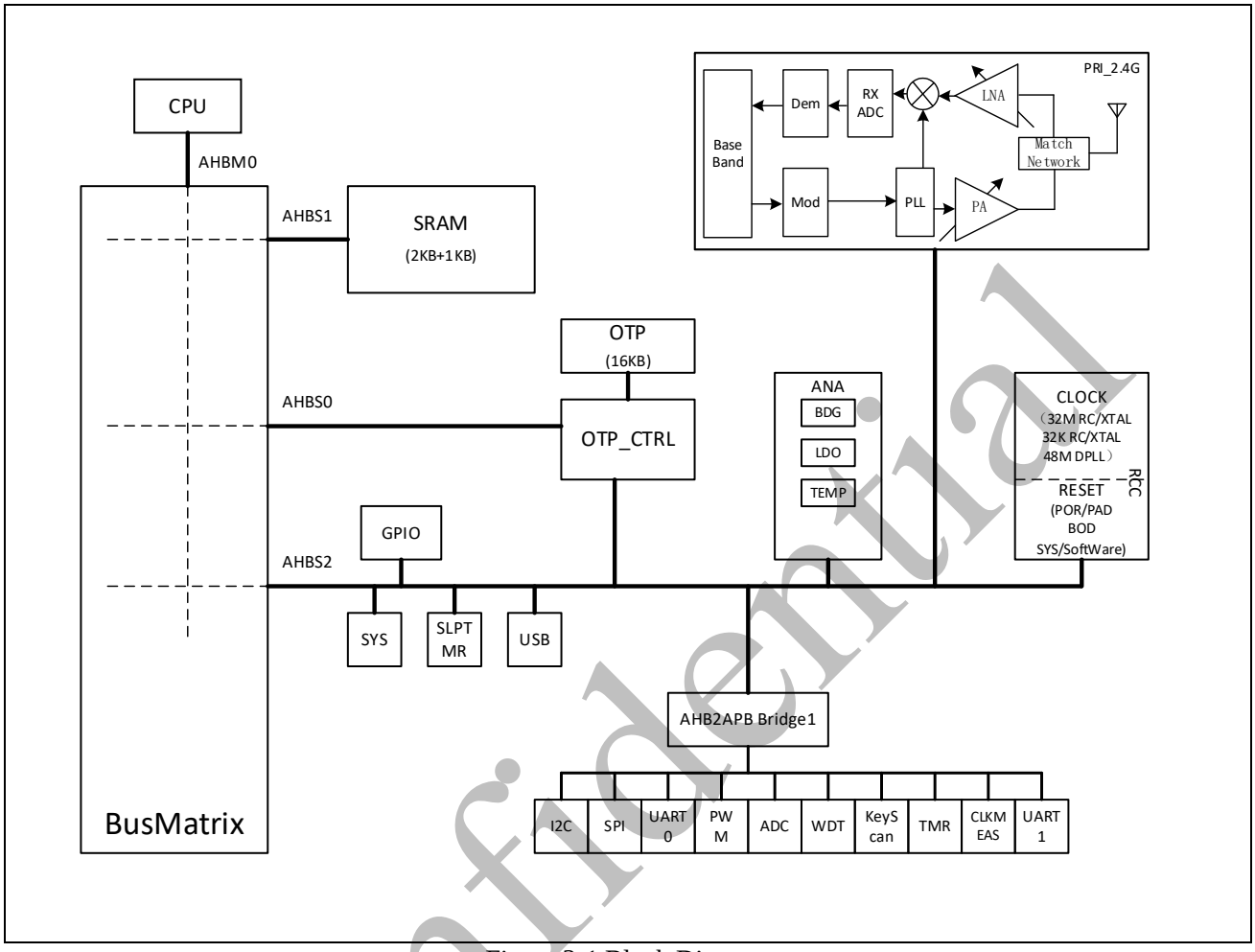


Figure 3-1 Block Diagram

4 Pin Information

4.1 SSOP24 Package

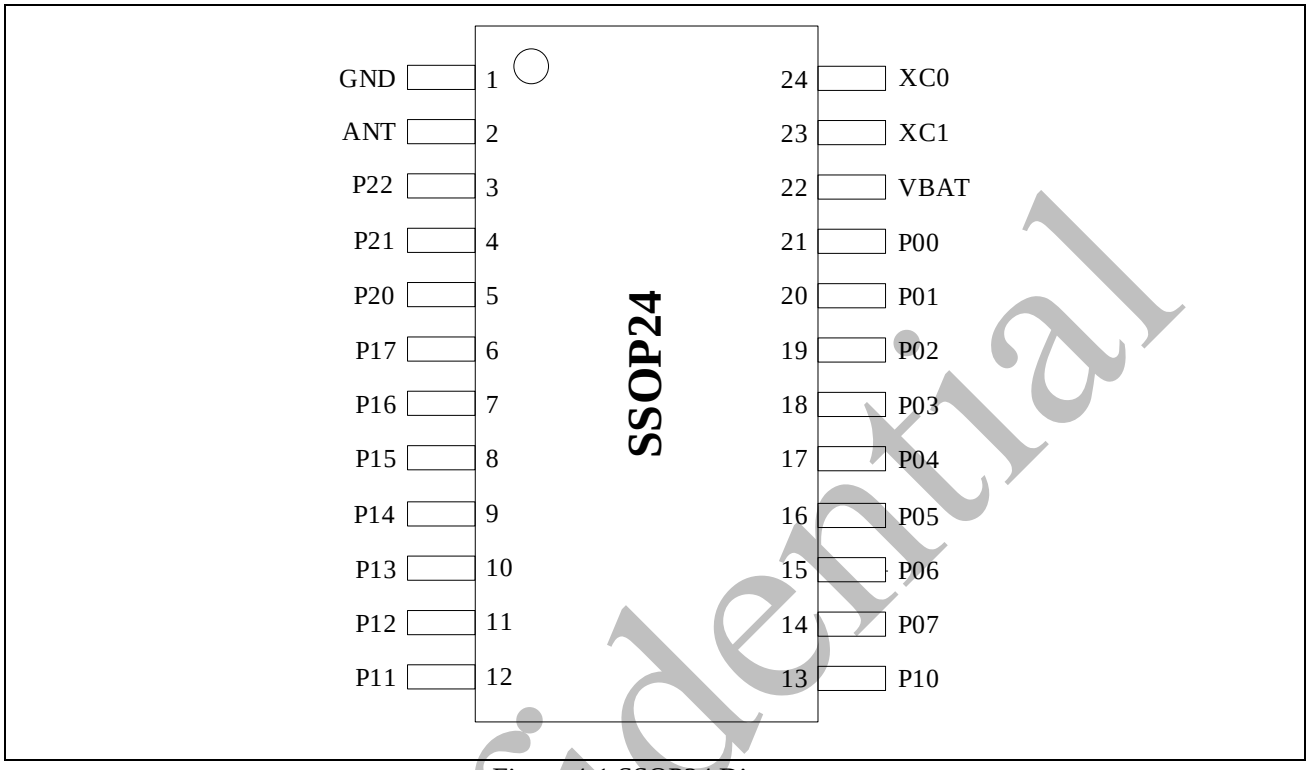


Figure 4-1 SSOP24 Diagram

Table 4-1 Pin Descriptions for SSOP24

Pin No. SSOP24	Pin Name	Pin Type	Description
1	GND	P	Ground (VSS)
2	ANT	AI/AO	RF antenna , an external antenna is required for use.
3[(1)]	P22	I/O	General-purpose digital input and output (The pull-up voltage must not exceed VBAT.)
	VPP	AI	OTP program VPP (6.25V~6.75V). Support input and open-drain output only. When used as an output pin, the IO port must be connected with a pull-up or pull-down resistor.
	KS_I0	I	Channel 0 keyscan input
	UART1_RX	I	UART1 RX
	EXT_STADC	I	ADC External pin trigger
	EXT_MEAS_CLK	I	External measurement clock
	TM0_EXT	I	Timer0 external input
	UART0_RX	I	UART0 RX

4	P21	I/O	General-purpose digital input and output
	ADC_CH21	AI	Channel 21 ADC input
	KS_O0	O	Channel 0 keyscan output
	UART1_RX	I	UART1 RX
	I2C0_SDA	I/O	I2C0 SDA
	XTL1	AI	External 32.768kHz clock source input
5	P20	I/O	General-purpose digital input and output
	ADC_CH20	AI	Channel 20 ADC input
	KS_I2	I	Channel 2 keyscan input
	UART1_TX	O	UART1 TX
	EXT_MEAS_CLK	I	External measurement clock
	XTL2	AO	External 32.768kHz clock source output
6	P17	I/O	General-purpose digital input and output
	ADC_CH17	AI	Channel 17 ADC input
	UART0_RX	I	UART0 RX
	PWM_CH1	O	Channel 1 PWM output
	KS_O4	O	Channel 4 keyscan output
7	P16	I/O	General-purpose digital input and output
	ADC_CH16	AI	Channel 16 ADC input
	UART0_TX	O	UART0 TX
	KS_I1	I	Channel 1 keyscan input
	PWM_CH0	O	Channel 0 PWM output
	I2C0_SCL	I/O	I2C0 SCL
8	P15	I/O	General-purpose digital input and output
	ADC_CH15	AI	Channel 15 ADC input
	SPI0_CS	I/O	SPI0 CS
	PWM_CH5	O	Channel 5 PWM output
	TM0_EXT	I	Timer0 external input
	UART0_RX	I	UART0 RX
	KS_O5	O	Channel 5 keyscan output
9	P14	I/O	General-purpose digital input and output
	ADC_CH14	AI	Channel 14 ADC input
	KS_O4	O	Channel 4 keyscan output

	I2C0_SCL	I/O	I2C0 SCL
	PWM_CH2	O	Channel 2 PWM output
	SPI0_CLK	I/O	SPI0 clock
	UART1_RX	I	UART1 RX
10	P13	I/O	General-purpose digital input and output
	ADC_CH13	AI	Channel 13 ADC input
	KS_O3	O	Channel 3 keyscan output
	I2C0_SDA	I/O	I2C0 SDA
	PWM_CH3	O	Channel 3 PWM output
	UART1_TX	O	UART1 TX
	SPI0_CS	I/O	SPI0 CS
11	P12	I/O	General-purpose digital input and output
	ADC_CH12	AI	Channel 12 ADC input
	UART0_RX	I	UART0 RX
	PWM_CH4	O	Channel 4 PWM output
	KS_O2	O	Channel 2 keyscan output
	SPI0_MISO	I/O	SPI0 MISO
12	P11	I/O	General-purpose digital input and output
	ADC_CH11	AI	Channel 11 ADC input
	KS_O1	O	Channel 1 keyscan output
	SPI0_MOSI	I/O	SPI0 MOSI
	EXT_MEAS_CLK	I	External measurement clock
	KS_I0	I	Channel 0 keyscan input
	UART0_TX	O	UART0 TX
13	P10	I/O	General-purpose digital input and output
	ADC_CH10	AI	Channel 10 ADC input
	KS_O0	O	Channel 0 keyscan output
	I2C0_SDA	I/O	I2C0 SDA
	SPI0_MISO	I/O	SPI0 MISO
	PWM_CH5	O	Channel 5 PWM output
14	P07	I/O	General-purpose digital input and output
	ADC_CH7	AI	Channel 7 ADC input
	KS_I5	I	Channel 5 keyscan input

	I2C0_SCL	I/O	I2C0 SCL
	SPI0_MOSI	I/O	SPI0 MOSI
	PWM_CH0	O	Channel 0 PWM output
15	P06	I/O	General-purpose digital input and output
	ADC_CH6	AI	Channel 6 ADC input
	KS_I4	I	Channel 4 keyscan input
	UART0_RX	I	UART0 RX
	SPI0_MISO	I/O	SPI0 MISO
	PWM_CH5	O	Channel 5 PWM output
16	P05	I/O	General-purpose digital input and output
	ADC_CH5	AI	Channel 5 ADC input
	KS_I3	I	Channel 3 keyscan input
	UART0_TX	O	UART0 TX
	SPI0_MISO	I/O	SPI0 MISO
	PWM_CH4	O	Channel 4 PWM output
17	P04	I/O	General-purpose digital input and output
	ADC_CH4	AI	Channel 4 ADC input
	KS_I2	I	Channel 2 keyscan input
	SPI0_CLK	I/O	SPI0 clock
	PWM_CH3	O	Channel 3 PWM output
	KS_O3	O	Channel 3 keyscan output
	UART1_RX	I	UART1 RX
18	P03	I/O	General-purpose digital input and output
	ADC_CH3	AI	Channel 3 ADC input
	KS_I1	I	Channel 1 keyscan input
	PWM_CH2	O	Channel 2 PWM output
	SPI0_CS	I/O	SPI0 CS
	UART1_TX	O	UART1 TX
	PIN RESET	I	Reset pin
19	P02	I/O	General-purpose digital input and output
	ADC_CH2	AI	Channel 2 ADC input
	KS_O1	O	Channel 1 keyscan output
	PWM_CH0	O	Channel 0 PWM output

	SPI0_MOSI	I/O	SPI0 MOSI
20[1]	P01	I/O	General-purpose digital input and output
	ADC_CH1	AI	Channel 1 ADC input
	SWD_DAT	I/O	SWD data input and output
	UART0_TX	O	UART0 TX
	I2C0_SDA	I/O	I2C0 SDA
	SPI0_CS	I/O	SPI0 CS
21[1]	P00	I/O	General-purpose digital input and output
	ADC_CH0	AI	Channel 0 ADC input
	SWD_CLK	I	SWD clock input
	UART0_RX	I	UART0 RX
	I2C0_SCL	I/O	I2C0 SCL
	SPI0_CLK	I/O	SPI0 clock
22	VBAT	P	Power input (VDD)
23	XC1	AO	External 32MHz clock source output
24	XC0	AI	External 32MHz clock source input

Note[1]: Pins for programming.

4.2 SOP16 / SOP14 Package

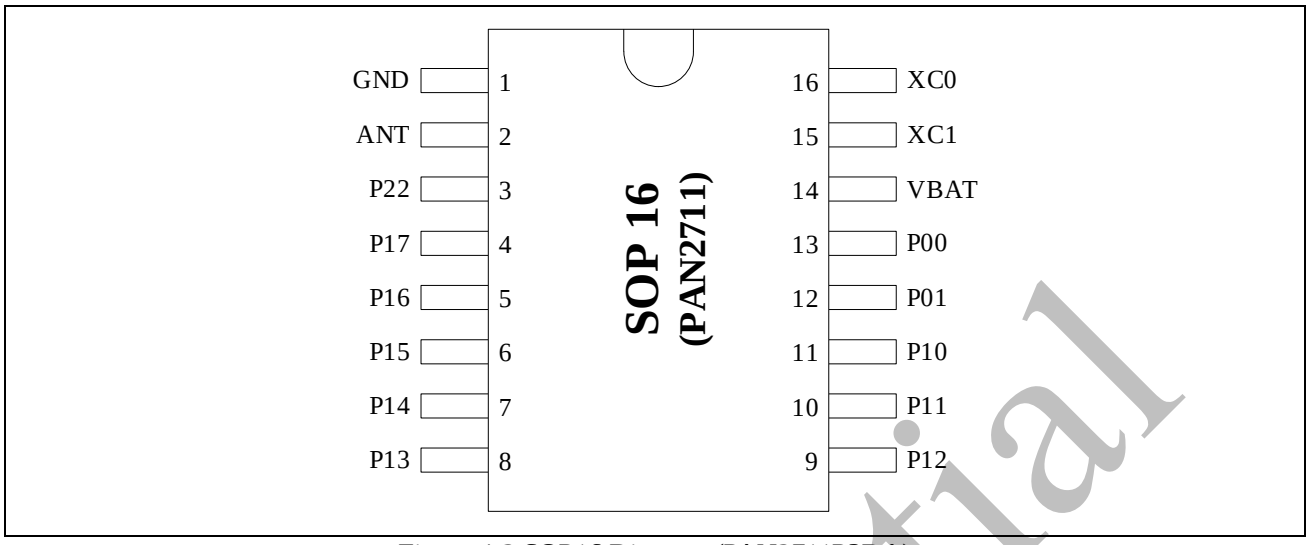


Figure 4-2 SOP16 Diagram (PAN2711P3DA)

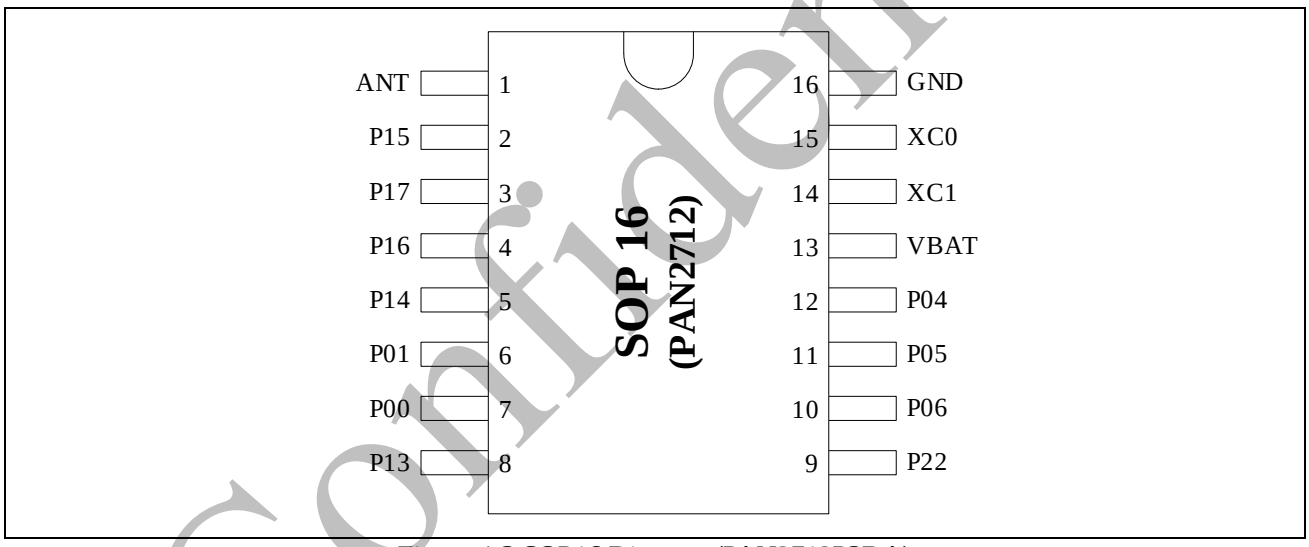


Figure 4-3 SOP16 Diagram (PAN2712P3DA)

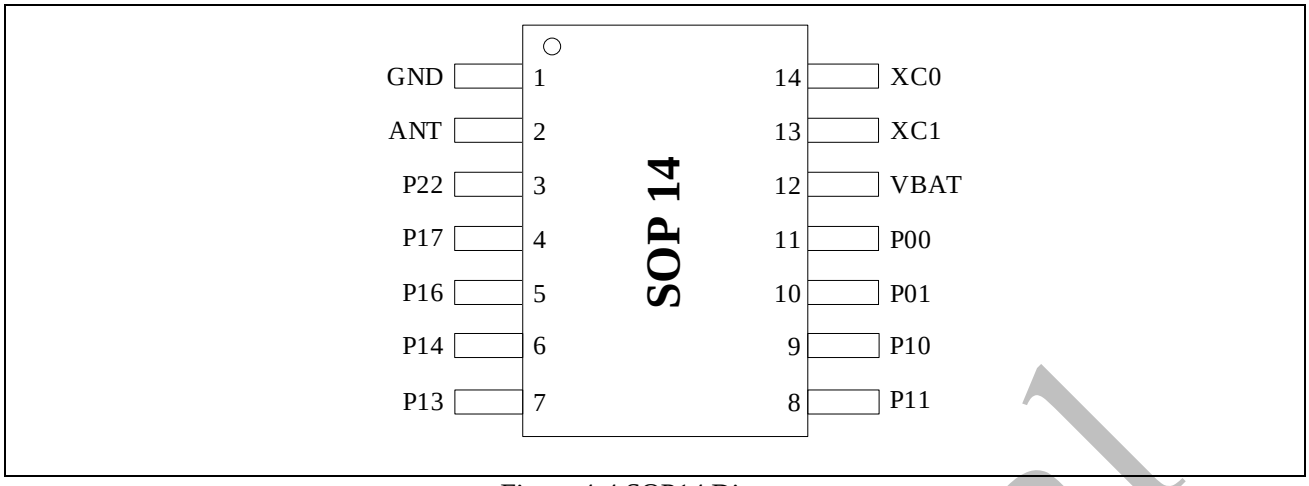


Figure 4-4 SOP14 Diagram

Table 4-2 Pin Descriptions for SOP16 and SOP14

Pin No.			Pin Name	Pin Type	Description
SOP16 (PAN2711)	SOP16 (PAN2712)	SOP14			
1	16	1	GND	P	Ground (VSS)
2	1	2	ANT	AI/AO	RF antenna , an external antenna is required for use.
3(1)	9(1)	3(1)	P22	I/O	General-purpose digital input and output (The pull-up voltage must not exceed VBAT.)
			VPP	AI	OTP program VPP (6.25V~6.75V). Support input and open-drain output only. When used as an output pin, the IO port must be connected with a pull-up or pull-down resistor.
			KS_I0	I	Channel 0 keyscan input
			UART1_RX	I	UART1 RX
			EXT_STADC	I	ADC External pin trigger
			EXT_MEAS_CLK	I	External measurement clock
			TM0_EXT	I	Timer0 external input
			UART0_RX	I	UART0 RX
4	3	4	P17	I/O	General-purpose digital input and output
			ADC_CH17	AI	Channel 17 ADC input
			UART0_RX	I	UART0 RX
			PWM_CH1	O	Channel 1 PWM output
			KS_O4	O	Channel 4 keyscan output
5	4	5	P16	I/O	General-purpose digital input and output
			ADC_CH16	AI	Channel 16 ADC input

			UART0_TX	O	UART0 TX
			KS_I1	I	Channel 1 keyscan input
			PWM_CH0	O	Channel 0 PWM output
			I2C0_SCL	I/O	I2C0 SCL
6	2	-	P15	I/O	General-purpose digital input and output
			ADC_CH15	AI	Channel 15 ADC input
			SPI0_CS	I/O	SPI0 CS
			PWM_CH5	O	Channel 5 PWM output
			TM0_EXT	I	Timer0 external input
			UART0_RX	I	UART0 RX
			KS_O5	O	Channel 5 keyscan output
7	5	6	P14	I/O	General-purpose digital input and output
			ADC_CH14	AI	Channel 14 ADC input
			KS_O4	O	Channel 4 keyscan output
			I2C0_SCL	I/O	I2C0 SCL
			PWM_CH2	O	Channel 2 PWM output
			SPI0_CLK	I/O	SPI0 clock
			UART1_RX	I	UART1 RX
8	8	7	P13	I/O	General-purpose digital input and output
			ADC_CH13	AI	Channel 13 ADC input
			KS_O3	O	Channel 3 keyscan output
			I2C0_SDA	I/O	I2C0 SDA
			PWM_CH3	O	Channel 3 PWM output
			UART1_TX	O	UART1 TX
			SPI0_CS	I/O	SPI0 CS
9	-	-	P12	I/O	General-purpose digital input and output
			ADC_CH12	AI	Channel 12 ADC input
			UART0_RX	I	UART0 RX
			PWM_CH4	O	Channel 4 PWM output
			KS_O2	O	Channel 2 keyscan output
			SPI0_MISO	I/O	SPI0 MISO
10	-	8	P11	I/O	General-purpose digital input and output
			ADC_CH11	AI	Channel 11 ADC input

			KS_O1	O	Channel 1 keyscan output
			SPI0_MOSI	I/O	SPI0 MOSI
			EXT_MEAS_CLK	I	External measurement clock
			KS_I0	I	Channel 0 keyscan input
			UART0_TX	O	UART0 TX
11	-	9	P10	I/O	General-purpose digital input and output
			ADC_CH10	AI	Channel 10 ADC input
			KS_O0	O	Channel 0 keyscan output
			I2C0_SDA	I/O	I2C0 SDA
			SPI0_MISO	I/O	SPI0 MISO
			PWM_CH5	O	Channel 5 PWM output
12(1)	6(1)	10(1)	P01	I/O	General-purpose digital input and output
			ADC_CH1	AI	Channel 1 ADC input
			SWD_DAT	I/O	SWD data input and output
			UART0_TX	O	UART0 TX
			I2C0_SDA	I/O	I2C0 SDA
			SPI0_CS	I/O	SPI0 CS
13(1)	7(1)	11(1)	P00	I/O	General-purpose digital input and output
			ADC_CH0	AI	Channel 0 ADC input
			SWD_CLK	I	SWD clock input
			UART0_RX	I	UART0 RX
			I2C0_SCL	I/O	I2C0 SCL
			SPI0_CLK	I/O	SPI0 clock
14	13	12	VBAT	P	Power input (VDD)
15	14	13	XC1	AO	External 32MHz clock source output
16	15	14	XC0	AI	External 32MHz clock source input
-	10	-	P06	I/O	General-purpose digital input and output
			ADC_CH6	AI	Channel 6 ADC input
			UART0_RX	I	UART0 RX
			SPI0_MISO	I/O	SPI0 MISO
			PWM_CH5	O	Channel 5 PWM output
			KS_I4	I	Channel 4 keyscan input
-	11	-	P05	I/O	General-purpose digital input and output

			ADC_CH5	AI	Channel 5 ADC input
			KS_I3	I	Channel 3 keyscan input
			UART0_TX	O	UART0 TX
			SPI0_MISO	I/O	SPI0 MISO
			PWM_CH4	O	Channel 4 PWM output
-	12	-	P04	I/O	General-purpose digital input and output
			ADC_CH4	AI	Channel 4 ADC input
			KS_I2	I	Channel 2 keyscan input
			SPI0_CLK	I/O	SPI0 clock
			PWM_CH3	O	Channel 3 PWM output
			KS_O3	O	Channel 3 keyscan output
			UART1_RX	I	UART1 RX

Note(1): Pins for programming.

4.3 MSOP10 Package

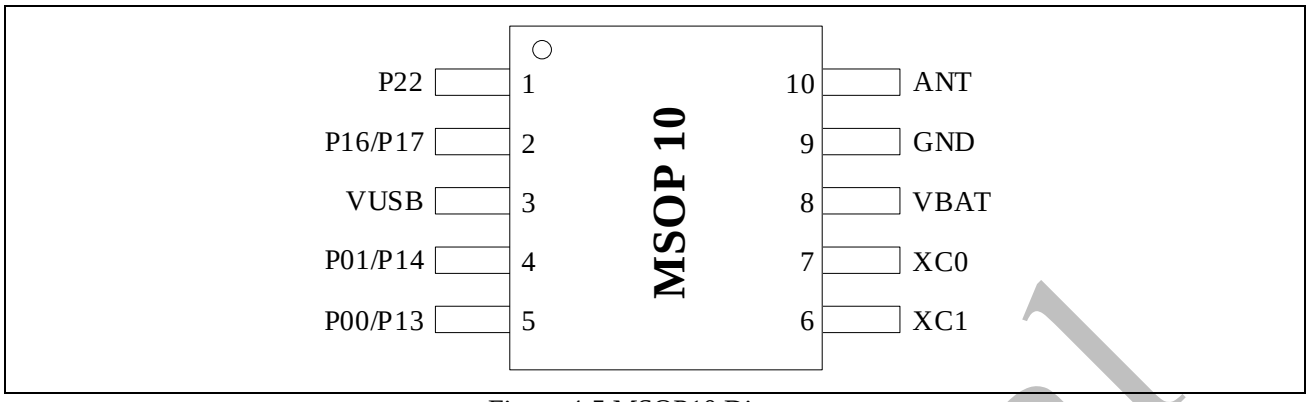


Figure 4-5 MSOP10 Diagram

Table 4-3 MSOP10 Pin Descriptions

Pin No. MSOP10	Pin Name	Pin Type	Description
1[1]	P22	I/O	General-purpose digital input and output (The pull-up voltage must not exceed VBAT.)
	VPP	AI	OTP program VPP (6.25V~6.75V). Support input and open-drain output only. When used as an output pin, the IO port must be connected with a pull-up or pull-down resistor.
	KS_I0	I	Channel 0 keyscan input
	UART1_RX	I	UART1 RX
	EXT_STADC	I	ADC External pin trigger
	EXT_MEAS_CLK	I	External measurement clock
	TM0_EXT	I	Timer0 external input
	UART0_RX	I	UART0 RX
2[2]	**P16**	**I/O**	**General-purpose digital input and output**
	ADC_CH16	AI	Channel 16 ADC input
	UART0_TX	O	UART0 TX
	KS_I1	I	Channel 1 keyscan input
	PWM_CH0	O	Channel 0 PWM output
	I2C0_SCL	I/O	I2C0 SCL
	P17	**I/O**	**General-purpose digital input and output**
	ADC_CH17	AI	Channel 17 ADC input
	UART0_RX	I	UART0 RX
	PWM_CH1	O	Channel 1 PWM output

	KS_O4	O	Channel 4 keyscan output
3	VUSB	P	USB 5V input
4[2]	**P01[1]**	**I/O**	**General-purpose digital input and output**
	ADC_CH1	AI	Channel 1 ADC input
	SWD_DAT	I/O	SWD data input and output
	UART0_TX	O	UART0 TX
	I2C0_SDA	I/O	I2C0 SDA
	SPI0_CS	I/O	SPI0 CS
	P14	**I/O**	**General-purpose digital input and output**
	ADC_CH14	AI	Channel 14 ADC input
	KS_O4	O	Channel 4 keyscan output
	I2C0_SCL	I/O	I2C0 SCL
	PWM_CH2	O	Channel 2 PWM output
	SPI0_CLK	I/O	SPI0 clock
	UART1_RX	I	UART1 RX
	USB_DP	AI/AO	USB dp
5[2]	**P00[1]**	**I/O**	**General-purpose digital input and output**
	ADC_CH0	AI	Channel 0 ADC input
	SWD_CLK	I	SWD clock input
	UART0_RX	I	UART0 RX
	I2C0_SCL	I/O	I2C0 SCL
	SPI0_CLK	I/O	SPI0 clock
	P13	**I/O**	**General-purpose digital input and output**
	ADC_CH13	AI	Channel 13 ADC input
	KS_O3	O	Channel 3 keyscan output
	I2C0_SDA	I/O	I2C0 SDA
	PWM_CH3	O	Channel 3 PWM output
	UART1_TX	O	UART1 TX
	SPI0_CS	I/O	SPI0 CS
	USB_DM	AI/AO	USB dm
6	XC1	AO	External 32MHz clock source output
7	XC0	AI	External 32MHz clock source input
8	VBAT	P	Power input (VDD)

9	GND	P	Ground (VSS)
10	ANT	AI/AO	RF antenna , an external antenna is required for use.

Note(1): Pins for programming.

Note(2): This pin has two sets of pads. You can choose any set of pads, but the other set must be in analog state.

4.4 Internal Connection

Table 4-4 Internal Connection for PAN2713M5BA

Pin Status	EEPROM	RF
I S	PAD_SDA	P10
I S	PAD_SCL	P07

5 Electrical Specification

Maximum and minimum values

In the notes below each table, the data obtained through comprehensive evaluation, design simulation and/or process features are not tested on the production line; based on the comprehensive evaluation, the minimum and maximum values are after the sample test. Take the average value and add and subtract three times the standard distribution (average ± 3 Σ).

5.1 RF Characteristics

Table 5-1 RF Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{OP}	Operating frequency		2400	-	2483	MHz
PLLres	PLL programming resolution		-	4	-	Hz
DR	Data rate		0.25	1	2	Mbps
$\Delta f_{BLE,2M}$	Frequency deviation @ BLE 2Mbps		-	500	-	kHz
$\Delta f_{BLE,1M}$	Frequency deviation @ BLE 1Mbps		-	250	-	kHz
$\Delta f_{BLE,250k}$	Frequency deviation @ BLE 250kbps		-	170	-	kHz
$\Delta f_{297,2M}$	Frequency deviation @ 297mode 2Mbps		-	500	-	kHz
$\Delta f_{297,1M}$	Frequency deviation @ 297mode 1Mbps		-	250	-	kHz
$\Delta f_{297,250k}$	Frequency deviation @ 297mode 250kbps		-	170	-	kHz
$\Delta f_{FS,2M}$	Frequency deviation @ FS-mode 2Mbps		-	320	-	kHz
$\Delta f_{FS,1M}$	Frequency deviation @ FS-mode 1Mbps		-	160	-	kHz
$\Delta f_{FS,250k}$	Frequency deviation @ FS-mode 250kbps		-	160	-	kHz
$f_{BLE,CS,2M}$	Channel spacing @ BLE 2Mbps		-	2	-	MHz
$f_{BLE,CS,1M}$	Channel spacing @ BLE 1Mbps		-	1	-	MHz
$f_{BLE,CS,250k}$	Channel spacing @ BLE 250kbps		-	1	-	MHz
$f_{297,CS,2M}$	Channel spacing @ 297mode 2Mbps		-	2	-	MHz
$f_{297,CS,1M}$	Channel spacing @ 297mode 1Mbps		-	1	-	MHz
$f_{297,CS,250k}$	Channel spacing @ 297mode 250kbps		-	1	-	MHz
$f_{FS,CS,2M}$	Channel spacing @ FS-mode 2Mbps		-	2	-	MHz
$f_{FS,CS,1M}$	Channel spacing @ FS-mode 1Mbps		-	1	-	MHz
$f_{FS,CS,250k}$	Channel spacing @ FS-mode 250kbps		-	1	-	MHz

Table 5-2 TX Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
P_{RFTX}	Output power		-55	-	11	dBm
P_{RFC}	RF power control range		-	66	-	dB
P_{RFCR}	RF power accuracy		-	-	±3	dB
$P_{RF1M,1}$	1st Adjacent Channel Transmit Power @1Mbps		-	33	-	dBc
$P_{RF1M,2}$	2nd Adjacent Channel Transmit Power @1Mbps		-	55	-	dBc
$P_{RF1M,\geqslant 3}$	3rd Adjacent Channel Transmit Power @1Mbps		-	65	-	dBc
$P_{RF2M,2}$	1st Adjacent Channel Transmit Power @2Mbps		-	33	-	dBc
$P_{RF2M,4}$	2nd Adjacent Channel Transmit Power @2Mbps		-	60	-	dBc
$P_{RF2M,\geqslant 6M}$	3rd Adjacent Channel Transmit Power @2Mbps		-	54	-	dBc
P_{BW1M}	20dB bandwidth @1Mbps		-	1.2	-	MHz
P_{BW2M}	20dB bandwidth @2Mbps		-	2.2	-	MHz
P_{BW250k}	20dB bandwidth @250kbps		-	1	-	MHz
$P_{SP,1}$	Spurious @$\leqslant$1GHz		-	-	-60	dBm
$P_{SP,2}$	Spurious @$\geqslant$1GHz		-	-	-40	dBm

Table 5-3 RX Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$P_{RX,MAX}$	Receive maximum input power		-	0	-	dBm
$P_{SENS,1M,BLE}$	Sensitivity, 1Mbps BLE	Sensitivity, 1Mbps ideal transmitter, ≤37 bytes, BER = 0.1% is presented.	-	-94	-	dBm
$P_{SENS,2M,BLE}$	Sensitivity, 2Mbps BLE		-	-91	-	dBm
$P_{SENS,125k,BLE}$	Sensitivity, 125kbps BLE		-	-100	-	dBm
$P_{SENS,500k,BLE}$	Sensitivity, 500kbps BLE		-	-98	-	dBm
$P_{SENS,250k}$	Sensitivity, 250kbps		-	-99	-	dBm
$P_{SENS,125k}$	Sensitivity, 125kbps		-	-102	-	dBm
$P_{SENS,32k}$	Sensitivity, 32kbps		-	-104	-	dBm
$P_{SENS,1M,297}$	Sensitivity, 1Mbps 297 mode		-	-94	-	dBm
$P_{SENS,2M,297}$	Sensitivity, 2Mbps 297 mode		-	-91	-	dBm
$P_{SENS,250k,297}$	Sensitivity, 250kbps 297 mode		-	-99	-	dBm
$P_{SENS,1M,FS}$	Sensitivity, 1Mbps FS-mode		-	-92	-	dBm
$P_{SENS,2M,FS}$	Sensitivity, 2Mbps FS-mode		-	-88	-	dBm
$P_{SENS,250k,FS}$	Sensitivity, 250kbps FS-mode		-	-98	-	dBm

$C/I_{CO,1M,BLE}$	Co-Channel interference@1Mbps		-	8	-	dB
$C/I_{1M,1M,BLE}$	Adjacent (1 MHz) interference@1Mbps		-	-8	-	dB
$C/I_{2M,1M,BLE}$	Adjacent (2 MHz) interference @1Mbps		-	-20	-	dB
$C/I_{\geq 3M,1M,BLE}$	Adjacent (≥3 MHz) interference @1Mbps		-	-33	-	dB
$C/I_{Image,1M,BLE}$	Image frequency interference @1Mbps		-	-19	-	dB
$C/I_{Image\pm 1M,1M,BLE}$	Adjacent (±1MHz) interference to in-band image frequency @1Mbps		-	-32	-	dB
$C/I_{\geq 6M,1M,BLE}$	Adjacent (≥6 MHz) interference @1Mbps		-	-46	-	dB
$C/I_{CO,2M,BLE}$	Co-Channel interference @2Mbps		-	8	-	dB
$C/I_{2M,2M,BLE}$	Adjacent (2 MHz) interference @2Mbps		-	-4	-	dB
$C/I_{4M,2M,BLE}$	Adjacent (4 MHz) interference @2Mbps		-	-40	-	dB
$C/I_{\geq 6M,2M,BLE}$	Adjacent (≥6 MHz) interference @2Mbps		-	-43	-	dB
$C/I_{Image,2M,BLE}$	Image frequency interference @2Mbps		-	-25	-	dB
$C/I_{Image\pm 2M,2M,BLE}$	Adjacent (±2 MHz) interference to in-band image frequency		-	-35	-	dB
$C/I_{\geq 12M,2M,BLE}$	Adjacent (≥12 MHz) interference @2Mbps		-	-48	-	dB

Table 5-4 RSSI Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$RSSI_{RFC}$	RSSI indication range		-90	-	-15	dBm
$RSSI_{Auu}$	RSSI accuracy		-	±2	-	dB
$RSSI_{Res}$	RSSI resolution		-	0.25	-	dB
$RSSI_{Per}$	RSSI Sample period		-	0.25	-	us

Table 5-5 RF Timing Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
TX Settling Time	The time required for the transmitter to transition from standby3 mode to a fully TX operational mode.	STB3→ TX ready	68	-	-	μs
RX Settling Time	The time required for the receiver to transition from standby3 mode to a fully RX operational mode.		57	-	-	μs
TX Exit Time	The time required for the transmitter to transition from transmitting mode to standby3 mode.		3	-	-	μs
RX Exit Time	The time required for the receiver to transition from receiving modeto standby3 mode.	RX→STB3	3	-	-	μs

TX-RX Transition Time	The time required to switch from TX to RX		56	-	-	μs
RX-TX Transition Time	The time required to switch from RX to TX		68	-	-	μs

Table 5-6 RF Power Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$I_{TX,P11dBm}$	TX only run current 11dBm		-	33	-	mA
$I_{TX,P10dBm}$	TX only run current 10dBm		-	29	-	mA
$I_{TX,P9dBm}$	TX only run current 9dBm		-	28	-	mA
$I_{TX,P8dBm}$	TX only run current 8dBm		-	26	-	mA
$I_{TX,P7dBm}$	TX only run current 7dBm		-	25	-	mA
$I_{TX,P6dBm}$	TX only run current 6dBm		-	23	-	mA
$I_{TX,P5dBm}$	TX only run current 5dBm		-	21	-	mA
$I_{TX,P4dBm}$	TX only run current 4dBm		-	29	-	mA
$I_{TX,P3dBm}$	TX only run current 3dBm		-	28	-	mA
$I_{TX,P2dBm}$	TX only run current 2dBm		-	26	-	mA
$I_{TX,P1dBm}$	TX only run current 1dBm		-	25	-	mA
$I_{TX,P0dBm}$	TX only run current 0dBm		-	10	-	mA
$I_{TX,P-4dBm}$	TX only run current -4dBm		-	9	-	mA
$I_{TX,P-8dBm}$	TX only run current -8dBm		-	7	-	mA
$I_{TX,P-14dBm}$	TX only run current -14dBm		-	5	-	mA
$I_{TX,P-21dBm}$	TX only run current -21dBm		-	4.5	-	mA
$I_{TX,P-31dBm}$	TX only run current -31dBm		-	4	-	mA
$I_{TX,P-55dBm}$	TX only run current -55dBm		-	3.5	-	mA
$I_{RX,1M}$	RX 1Mbps current		-	7	-	mA
$I_{RX,2M}$	RX 2Mbps current		-	7.5	-	mA
$I_{RX,250k}$	RX 250kbps current		-	6.8	-	mA

Test conditions and methods.
1. The power consumption tested is the RF peak power.
2. The test method uses the total power consumption minus the power consumption of the MCU when the RF is not operating to calculate the final power consumption.
3. 3.3V Power Supply

5.2 GPIO Characteristics

Table 5-7 GPIO Characteristics (Single IO)

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{IH}	Input high voltage	T_A=25°C	0.65*VDD	-	VDD	V
V_{IL}	Input low voltage	Load capacitance =20pF, T_A=25°C	VSS	-	VSS+0.3*VDD	V
I_{Lkg}	Leakage current, open-drain mode or input mode	VDD≤VIN≤3.6V	-	6	-	nA
R_{PU}	Pull-up resistor	Vin =VSS，VDD =3.3V	-	48	-	kΩ
R_{PD}	Pull-down resistor	Vin =VSS，VDD =3.3V	-	92	-	kΩ
V_I	Input voltage	T_A=25°C	VSS	-	VDD	V
V_O	Output voltage	T_A=25°C	VSS	-	VDD	V
I_{OH}	Source current (Push-pull output)	Vin =VDD-0.5V	1.7	1.7	11.8	mA
I_{OL}	Sink current (Push-pull output)	Vin =VSS+0.5V, T_A=25°C	2.1	2.1	13.7	mA
I_{OL*}	Sink current (Push-pull output)	Vin =VSS+0.5V, T_A=25°C	46	46	57	mA
f_{Port_CLK}	IO output frequency	Load capacitance =10pF	-	-	48	MHz

Note: The GPIOs of P1x

Table 5-8 Combined Test

Description	Conditions	Status	Remark
IO default state after power on	VDD=3.3V ,T_A=25°C	P00, P01, P03: Pull-up input state Others: High resistance state	
IO status in deepsleep mode	VDD=3.3V ,T_A=25°C	All GPIOs can be configured	Cannot float in input state
IO status at reset	VDD=3.3V ,T_A=25°C	P00, P01, P03: Pull-up input state Others: High resistance state	

Table 5-9 nRESET Input Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{ILR}	Negative threshold voltage, nRESET	VDD=1.8V-3.3V , T_A=25°C	-	-	0.3*VDD	V
V_{IHR}	Positive threshold voltage, nRESET	VDD=1.8V-3.3V , T_A=25°C	0.65*VDD	-	-	V
V_{hys_rst}	Schmitt Trigger Voltage Hysteresis	VDD=1.8V-3.3V , T_A=25°C	-	-	0.35*VDD	V
R_{RST}	nRESET pin internal pull-up resistor	VDD=3.3V, T_A=25°C	-	48	-	kΩ

$t_{FR,\ 0.3pF}$	nRESET pin input filter pulse time	VDD=3.3V, T_A=25°C	-	TBD	-	ns

5.3 Reset Characteristics

Table 5-10 Reset Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
V_{BOD}	Brown-out detection voltage threshold	BODSEL<2:0> = 000, BOD_VSEL=00000(falling edge), dVDD/dt≤3V/s	-	1.85	-	V
		BODSEL<2:0> = 001, BOD_VSEL=00000(falling edge), dVDD/dt≤3V/s	-	1.93	-	
		BODSEL<2:0> = 010, BOD_VSEL=00000(falling edge), dVDD/dt≤3V/s	-	2.03	-	
		BODSEL<2:0> = 011, BOD_VSEL=00000(falling edge), dVDD/dt≤3V/s	-	2.12	-	
		BODSEL<2:0> = 100, BOD_VSEL=00000(falling edge), dVDD/dt≤3V/s	-	2.21	-	
		BODSEL<2:0> = 101, BOD_VSEL=00000(falling edge), dVDD/dt≤3V/s	-	2.32	-	
		BODSEL<2:0> = 110, BOD_VSEL=00000(falling edge), dVDD/dt≤3V/s	-	2.43	-	
		BODSEL<2:0> = 111, BOD_VSEL=00001(falling edge), dVDD/dt≤3V/s	-	2.52	-	
		BODSEL<2:0> = 111, BOD_VSEL=00011(falling edge), dVDD/dt≤3V/s	-	2.58	-	
		BODSEL<2:0> = 111, BOD_VSEL=00111(falling edge), dVDD/dt≤3V/s	-	2.66	-	
		BODSEL<2:0> = 111, BOD_VSEL=01111(falling edge), dVDD/dt≤3V/s	-	2.71	-	
		BODSEL<2:0> = 111, BOD_VSEL=11111(falling edge), dVDD/dt≤3V/s	-	2.8	-	
V_{BODhys}	BOD hysteresis voltage	dVDD/dt≤3V/s	65	-	111	mV

T_{BOD_RE1}	BOD response Time(Normal mode)	dVDD/dt≤3V/s	1	32	32	1/SLOW_CLK
I_{BOD}	BOD operating current	dVDD/dt≤3V/s	-	620	-	μA
V_{POR}	Power on reset voltage threshold	Rising edge, dVDD/dt≤3V/s	-	1.73	-	V
		Falling edge, dVDD/dt≤3V/s	-	1.65	-	V
T_{POR}	POR settling time	VDD =3.3V	-	1.2	-	ms
V_{LVR}	LVR detection voltage threshold	Falling edge, dVDD/dt≤3V/s	-	1.74	-	V
T_{LVR_RE}	LVR response time	T_A=25°C, dVDD/dt≤3V/s	1	32	32	1/SLOW_CLK
I_{LVR}	LVR operating current	T_A=25°C, dVDD/dt≤3V/s	-	500	-	μA

5.4 Clock Characteristics

Table 5-11 32MHz HXTAL Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{HXTL}	High speed crystal oscillator (HXTAL) frequency	VDD=3.3V ,T_A=25°C	-	32	-	MHz
$C_{LoadHXTL}$	Crystal load capacitance	VDD=3.3V ,T_A=25°C	-	10	-	pF
I_{DDHXTL}	HXTAL oscillator operating current	VDD=3.3V ,T_A=25°C	-	410	-	μA
t_{SUHXTL}	HXTAL oscillator startup time	VDD=3.3V ,T_A=25°C, ESR=40Ω, C_{HXTL}= 12pF	-	270	-	μs
$t_{SUHXTL\ Quick}$	HXTAL oscillator Quick startup time	VDD=3.3V ,T_A=25°C, ESR=40Ω, C_{HXTL}= 12pF	-	85	-	μs
ESR_{HXTL}	Equivalent series resistance	VDD=3.3V ,T_A=25°C	-	40	-	Ω
$F_{TOLHXTL}$	Frequency tolerance for the crystal	VDD=3.3V ,T_A=25°C	-20	-	20	ppm
PD_{HXTL}	Drive level	VDD=3.3V ,T_A=25°C	-	-	100	μW

Table 5-12 16MHz HXTAL Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{HXTL}	High speed crystal oscillator (HXTAL) frequency	VDD=3.3V ,T_A=25°C	-	16	-	MHz
$C_{LoadHXTL}$	Crystal load capacitance	VDD=3.3V ,T_A=25°C	-	10	-	pF
I_{DDHXTL}	HXTAL oscillator operating current	VDD=3.3V ,T_A=25°C	-	318	-	μA
t_{SUHXTL}	HXTAL oscillator startup time	VDD=3.3V ,T_A=25°C, ESR=40Ω, C_{HXTL}= 12pF	-	592	-	μs
$t_{SUHXTL\ Quick}$	HXTAL oscillator Quick startup time	VDD=3.3V ,T_A=25°C, ESR=40Ω, C_{HXTL}= 12pF	-	140	-	μs
ESR_{HXTL}	Equivalent series resistance	VDD=3.3V ,T_A=25°C	-	60	-	Ω
$F_{TOLHXTL}$	Frequency tolerance for the crystal	VDD=3.3V ,T_A=25°C	-20	-	20	ppm
PD_{HXTL}	Drive level	VDD=3.3V ,T_A=25°C	-	-	100	μW

Table 5-13 32.768kHz LXTAL Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{LXTL}	Low speed crystal oscillator (LXTAL) frequency	VDD=3.3V ,T_A=25°C	-	32.768	-	kHz
$C_{LoadLXTL}$	Crystal load capacitance	VDD=3.3V ,T_A=25°C	-	12.5	-	pF
I_{DDLXTL}	LXTAL oscillator operating current	VDD=3.3V ,T_A=25°C	-	420	-	nA
t_{SULXTL}	LXTAL oscillator Normal startup time	VDD=3.3V ,T_A=25°C	-	599	-	ms
$t_{SULXTL\ Quick}$	LXTAL oscillator Quick startup time	VDD=3.3V ,T_A=25°C	-	63	-	ms
ESR_{LXTL}	Equivalent series resistance	VDD=3.3V ,T_A=25°C	-	-	70	kΩ
PD_{LXTL}	Drive level	VDD=3.3V ,T_A=25°C	-	0.1	0.5	μW

Table 5-14 32MHz RCH Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{IRC32M}	Crystal frequency	VDD=3.3V ,T_A=25°C	-	32	-	MHz
ACC_{IRC32M}	Frequency accuracy	VDD=3.3V, T_A=-40°C to +105°C	-	-	-	%
		VDD=3.3V, T_A=-20°C to +85°C	-	-	-	%
		VDD=3.3V, T_A=25°C	-	±1	-	%
D_{IRC32M}	IRC32M oscillator duty cycle	VDD=3.3V, f_{IRC32M}=32MHz, T_A=25°C	49	51	53	%
$I_{DDIRC32M}$	Operating current	VDD=3.3V, f_{IRC32M}=32MHz, T_A=25°C	-	82	-	μA
$t_{SUIRC32M}$	Startup time	VDD=3.3V, f_{IRC32M}=32MHz, T_A=25°C	-	5	-	μs
$d_{fIRC32M}$	25°C, the frequency drifts with the supply voltage	VDD=1.8V to 3.6V, T_A=25°C	-	0.7	-	%/V

Table 5-15 32.768kHz RCL Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{IRC32K}	Crystal frequency	VDD=3.3V ,T_A=25°C	-	32.768	-	kHz
ACC_{IRC32K}	Frequency accuracy	VDD=3.3V, T_A=40°C to +105°C (After calibration)	-	-	-	%
		VDD=3.3V, T_A=25°C (After calibration)	-	±500	-	ppm
D_{IRC32K}	IRC32K oscillator duty cycle	VDD=3.3V, f_{IRC32K}=32.768kHz, T_A=25°C	49	51	53	%
$I_{DDIRC32K}$	Operating current	VDD=3.3V, f_{IRC32K}=32.768kHz,	-	310	-	nA

		T_A=25°C				
$t_{SUIRC32K}$	Startup time	VDD=3.3V, f_{IRC32K}=32.768kHz, T_A=25°C	-	480	-	μs
df_{IRC32K}	25°C, The frequency drifts with the supply voltage	VDD=1.8V to 3.6V, T_A=25°C	-	0.3	-	%/V

Table 5-16 DPLL Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
f_{PLLIN}	PLL input clock frequency	VDD=3.3V, T_A=25°C	16	32	-	MHz
f_{PLL}	PLL output clock frequency	VDD=3.3V, T_A=25°C	-	32	48	MHz
I_{PLL}	Operating current	VDD=3.3V, T_A=25°C	-	570	-	μA

5.5 ADC Characteristics

Table 5-17 Power Supply and Input Range Conditions

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
$V_{Ax(VBG\ adc)}$	Analog input voltage range，VBG（1.2V）	VDD=3.3V, T_A=25°C	0	-	1.2	V
$V_{Ax(VDD)}$	Analog input voltage range，VDD	VDD=3.3V, T_A=25°C	0	-	VDD	V
$I_{ADC(VBG\ mode)}$	ADC supply current	VDD=3.3V, TA=25°C Fadc = 1MHz	-	0.41	-	mA
$I_{ADC(VDD\ mode)}$	ADC supply current	VDD=3.3V, TA=25°C Fadc = 1MHz	-	0.56	-	mA

Table 5-18 ADC Built-in Voltage Reference

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VBG_{ADC}	Internal 1.2V Reference Voltage	VDD=3.3V, T_A=25°C	1.19	1.2	1.21	V
T_{Coef}	Temperature factor	T_A=-40°C to 105°C; VDD=1.8V to 3.6V	-	30	-	ppm/°C

Table 5-19 Time Parameters

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
F_{ADC}	ADC clock frequency	VDD=3.3V, T_A=25°C	0.256	1	2	MHz

Table 5-20 Linearity Parameter

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
INL	Integral linearity error	VDD=3.3V, T_A=25°C	-	-	±1.5	LSB
DNL	Differential linearity error	VDD=3.3V, T_A=25°C	-	-	±1	LSB
SNR	Signal to Noise Ratio	Fadc = 1MHz Input Clock 20kHz VDD=3.3V, T_A=25°C	-	69	-	dB
THD	Total harmonic distortion		-	-75	-	dB
SFDR	Spurious-free signal dynamic range		-	80	-	dB
ENOB	Effective number of bits		-	11	-	Bit

5.6 General Operating Conditions

Table 5-21 General Operating Conditions

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VDD*	Operating voltage	-	1.8	-	3.8	V
VUSB	Operating voltage	-	4.5	-	5.5	V
T_{ST}	Storage temperature	-	-65	-	150	℃
T_A	Ambient temperature	-	-40	-	85	℃
$T_{J\text{-}MSOP10}$	Junction temperature	MSOP10	-40	-	125	℃
$T_{J\text{-}SOP16}$	Junction temperature	SOP16	-40	-	125	℃
$R_{\theta JA\text{-}MSOP10}$	Thermal resistance	MSOP10	-	-	-	℃/W
$R_{\theta JA\text{-}SOP16}$	Thermal resistance	SOP16	-	-	-	℃/W

Note: VDD = VBAT

5.7 ESD Characteristics

Table 5-22 ESD Characteristics

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VESDHBM[1]	ESD @ Human Body Mode	T_A=25°C	-	±2000	-	V
VESDCDM[2]	ESD @ Charge Device Mode	T_A=25°C	-	±2000	-	V
VESDMM[3]	ESD @ Machine Mode	T_A=25°C	-	±200	-	V
$I_{latchup}$[4]	Latch up current	T_A=25°C	-	±100	-	mA

Notes:

1. Determined by ANSI/ESDA/JEDEC JS-001 standard, Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) - Device Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 Electrostatic Discharge Sensitivity (ESD) Test

Standard.

3. Determined according to JESD22-A115-C electrostatic discharge sensitivity (ESD) test standard.
4. Determined according to JEDEC EIA/JESD78 standard.

5.8 Absolute Maximum Ratings

Table 5-23 Absolute Maximum Ratings

Symbol	Description	Conditions	Parameter			Unit
			Min	Typ	Max	
VDD[1]-VSS	Supply voltages	T_A=25°C	-0.3	-	3.8	V
VIN	I/O pin voltage	T_A=25°C	VSS[2]-0.3	-	VDD+0.3	V
PVDD	Extreme power consumption	VDD=3.3V, T_A=25°C DCDC power supply	-	166.78	-	mW

Notes:

1. VDD = VBAT
2. VSS = GND

5.9 MCU Current Characteristics

Symbol	Conditions	Clock Source	AHB Division	CPU Freq	OTP Division	OTP Freq	VBAT	Current	Power
				(MHz)	-	(MHz)	(V)	(mA)	(mW)
Run mode	All peripherals clock on, run while(1) in OTP	RCH .cal 32M	2	16	2	8	3.3	2.52	8.316
			1	32	2	16	3.3	3.36	11.088
		XTH .off rch	2	16	2	8	3.3	2.44	8.052
			1	32	2	16	3.3	3.27	10.791
		DPLL 32M .ref rch	2	16	2	8	3.3	3.06	10.098
			1	32	2	16	3.3	3.92	12.936
		DPLL 48M .ref rch	2	24	2	12	3.3	3.53	11.649
			1	48	3	16	3.3	4.5	14.85
		DPLL 32M .ref xth	2	16	2	8	3.3	2.93	9.669
			1	32	2	16	3.3	3.77	12.441
		DPLL 48M .ref xth	2	24	2	12	3.3	3.39	11.187
			1	48	3	16	3.3	4.36	14.388
	All peripherals clock off, run while(1) in OTP	RCH .cal 32M	2	16	2	8	3.3	2.01	6.633
			1	32	2	16	3.3	2.53	8.349
		XTH .off rch	2	16	2	8	3.3	1.94	6.402
			1	32	2	16	3.3	2.46	8.118
		DPLL 32M .ref rch	2	16	2	8	3.3	2.18	7.194
			1	32	2	16	3.3	2.71	8.943
		DPLL 48M .ref rch	2	24	2	12	3.3	2.49	8.217
			1	48	3	16	3.3	2.96	9.768

		DPLL 32M .ref xth	2	16	2	8	3.3	2.05	6.765
			1	32	2	16	3.3	2.57	8.481
		DPLL 48M .ref xth	2	24	2	12	3.3	2.36	7.788
			1	48	3	16	3.3	2.83	9.339

Note: The above are all typical values.

Symbol	Conditions	SLP_AHB_CLK_DIV	CPU Freq (MHz)	OTP Division	OTP Freq (MHz)	Total Power (mA)
Sleep mode	Sleep all peripheral on	f	32	2	16	1.24
		7	32	2	16	1.28
		0	32	2	16	1.83
	Sleep all peripheral off	f	32	2	16	1
		7	32	2	16	1.01
		0	32	2	16	1.08

Symbol	Conditions	Power (μA)
Deepsleep	Wake by GPIO(edge)/32k/all retention	1.68
	Wake by GPIO/all retention	1.44
	Wake by 32k/all retention	1.65
Standby m1	Wake by GPIO/3K SRAM retention	1.33
	Wake by 32k/3K SRAM retention	1.12
Standby m0	Wake by GPIO	0.82

6 Application Reference Diagram

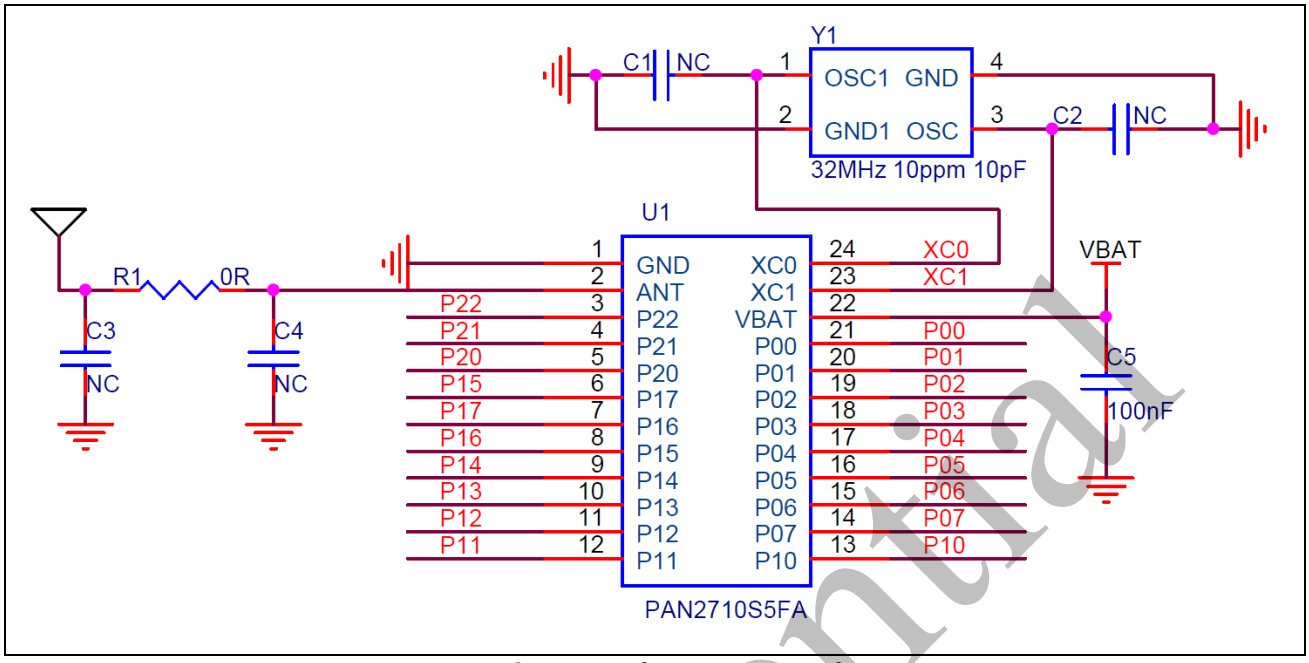


Figure 6-1 Application Reference Diagram for SSOP24

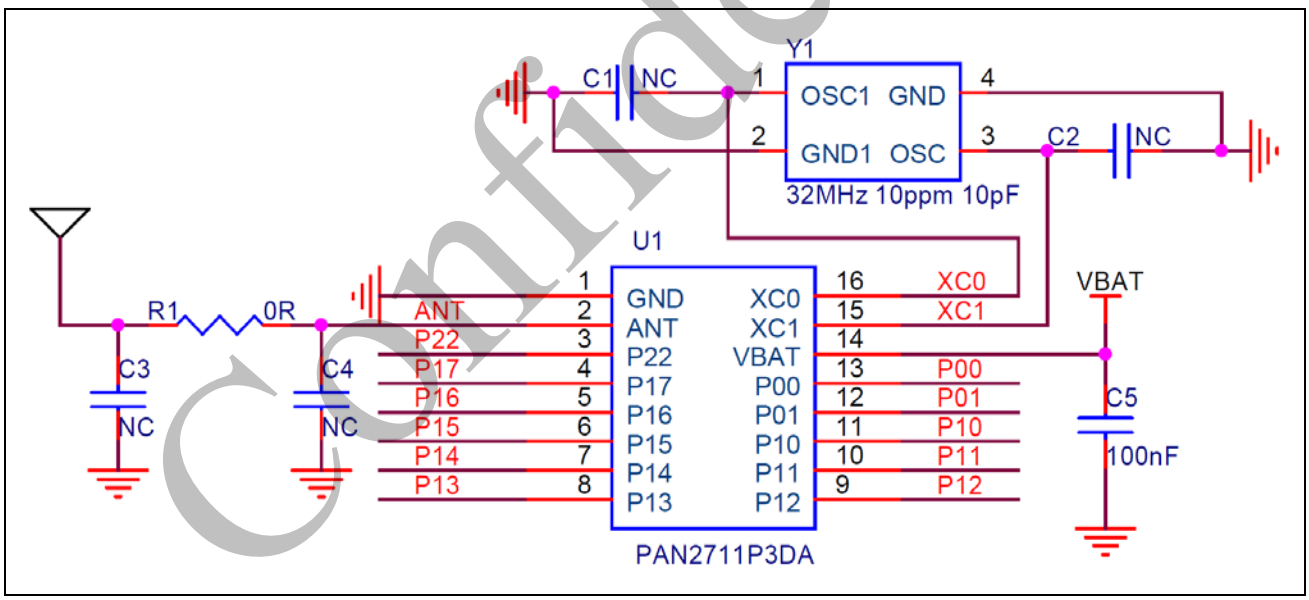


Figure 6-2 Application Reference Diagram for SOP16 (PAN2711P3DA)

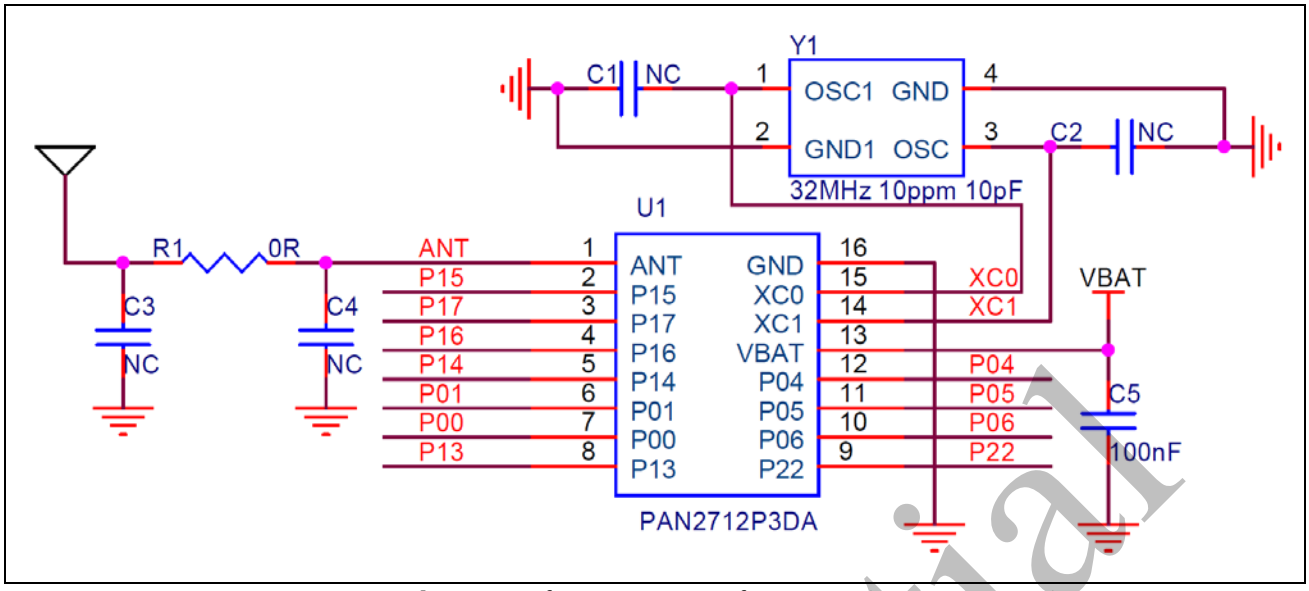


Figure 6-3 Application Reference Diagram for SOP16 (PAN2712P3DA)

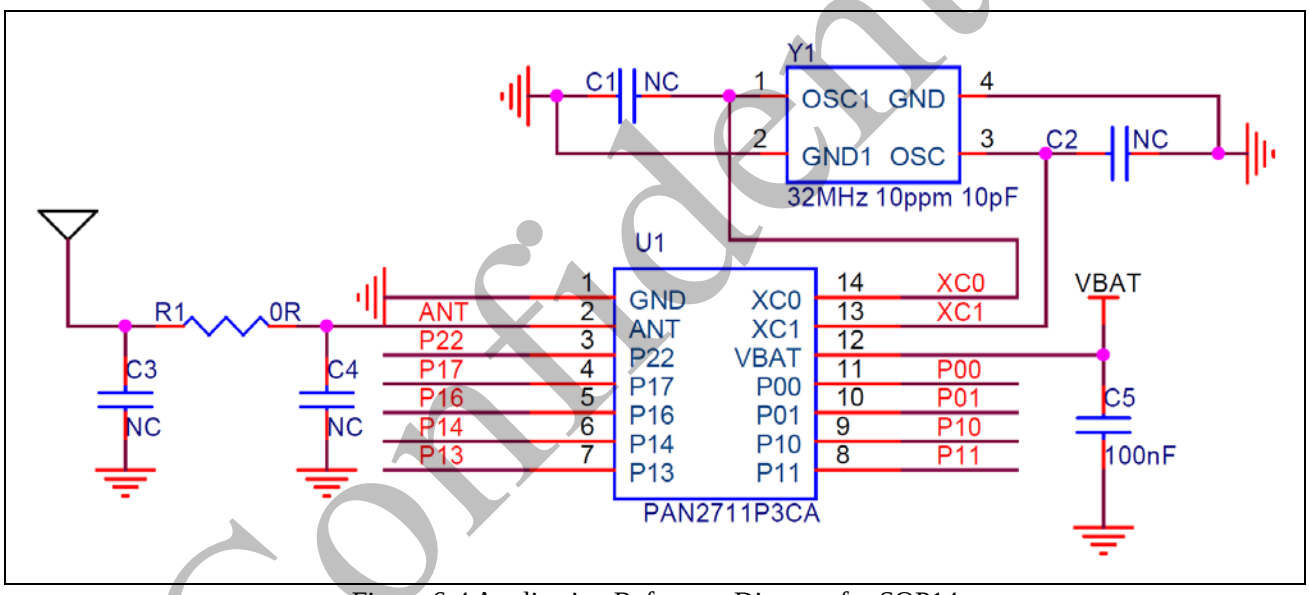


Figure 6-4 Application Reference Diagram for SOP14

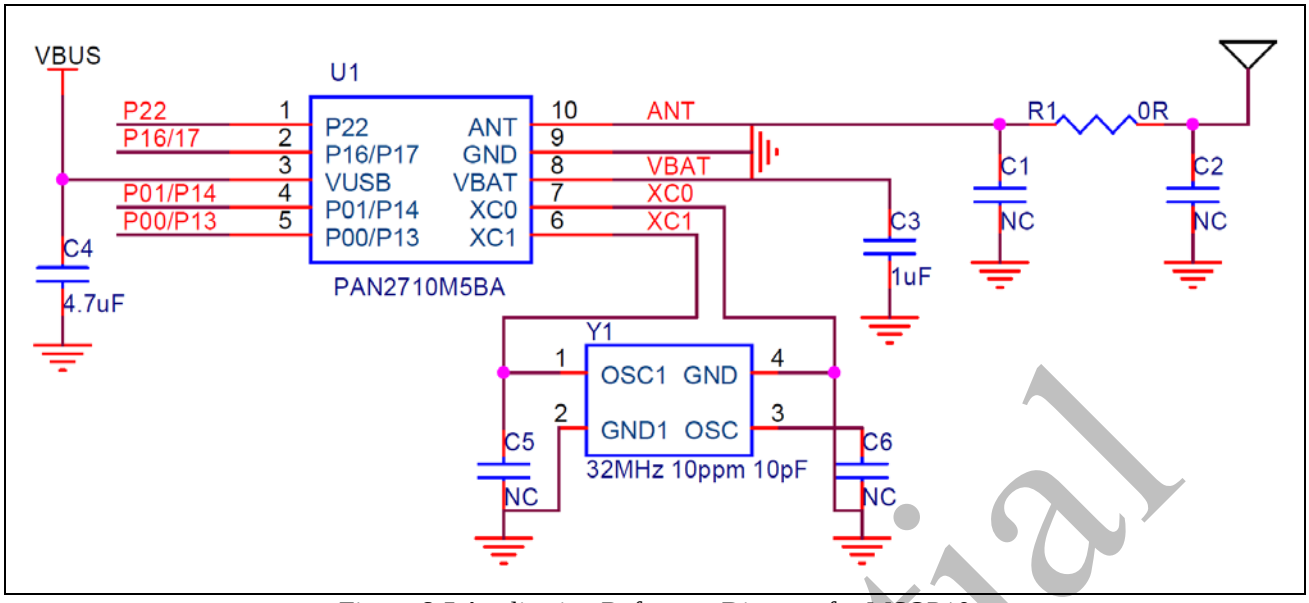


Figure 6-5 Application Reference Diagram for MSOP10

7 Package Dimensions

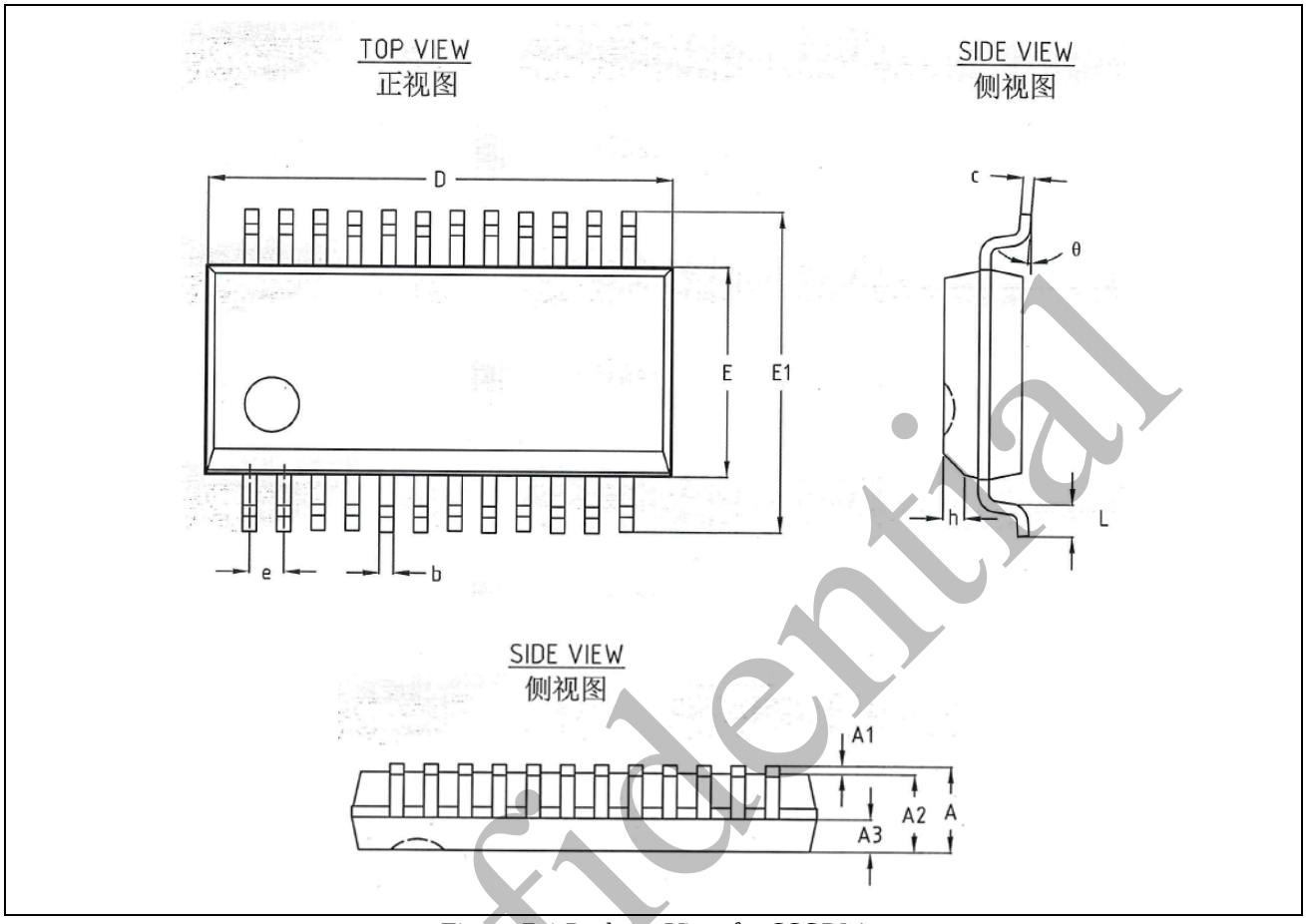


Figure 7-1 Package View for SSOP24

Table 7-1 Package Dimension for SSOP24

SYMBOL	MIN（mm）	NOM（mm）	MAX（mm）
A	-	-	1.750
A1	0.040	-	0.250
A2	1.350	1.450	1.550
A3	0.600	0.650	0.700
b	0.203	-	0.310
c	0.102	-	0.254
D	8.450	-	8.850
E	3.800	3.900	4.000
E1	5.800	6.000	6.200
e	0.635 BSC		
h	0.300	-	0.500
L	0.400	-	0.800
Ø	0	-	8°

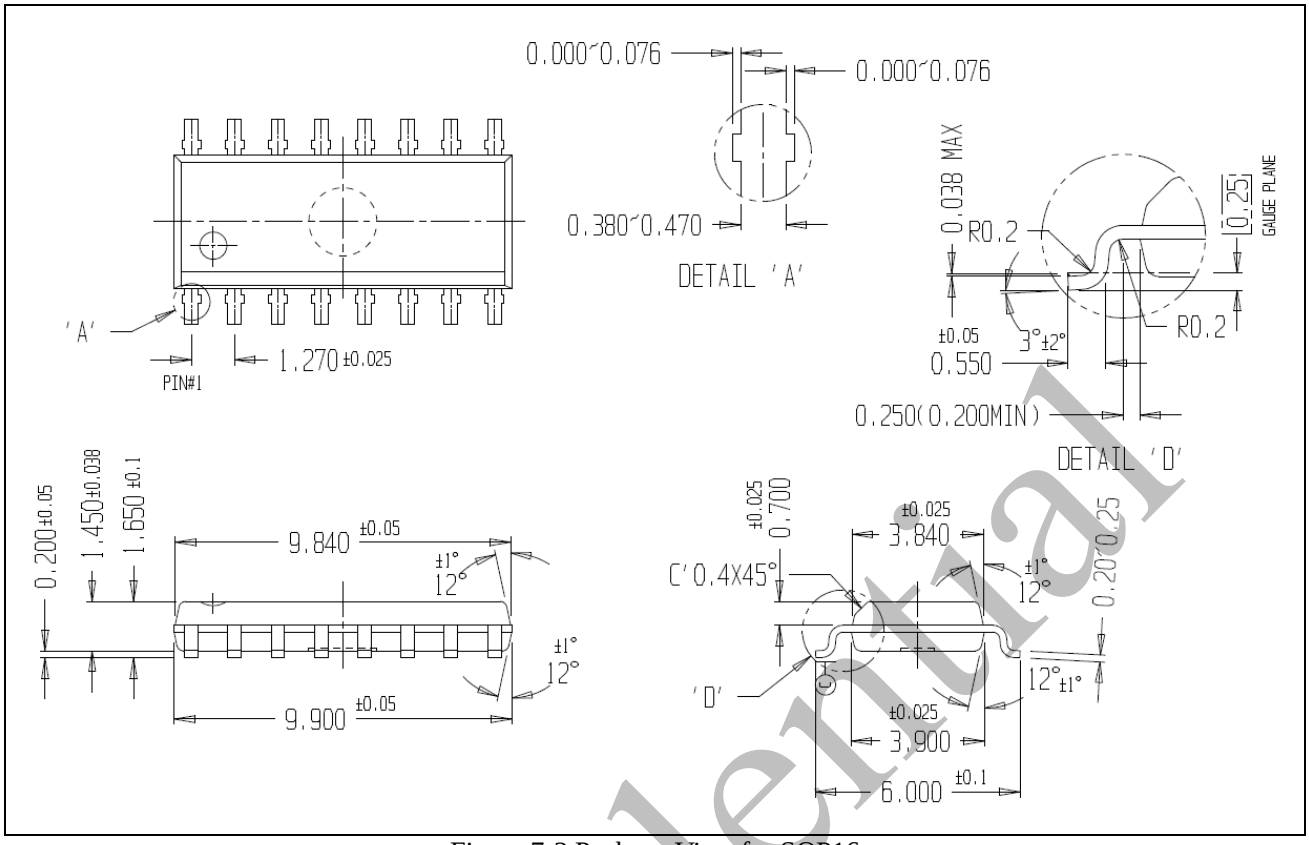


Figure 7-2 Package View for SOP16

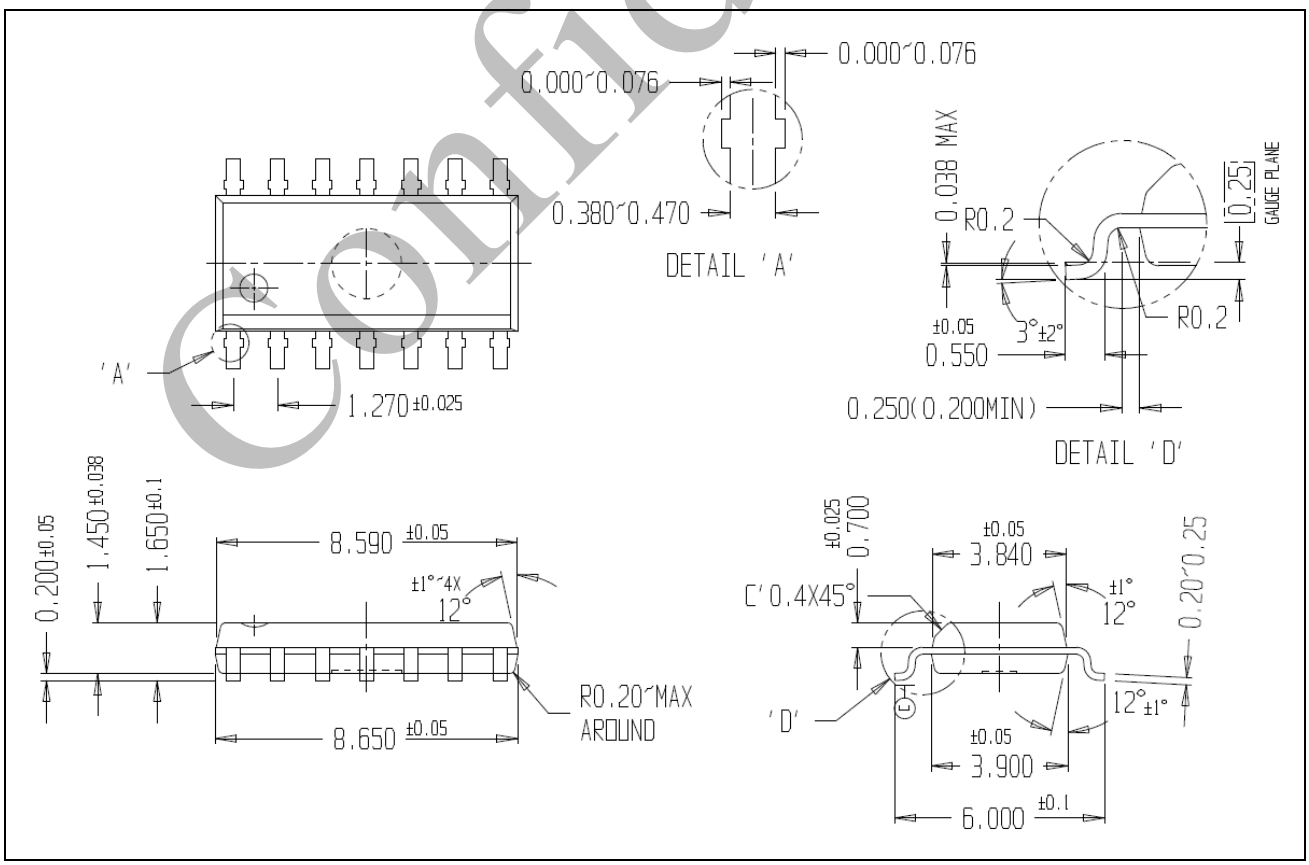


Figure 7-3 Package View for SOP14

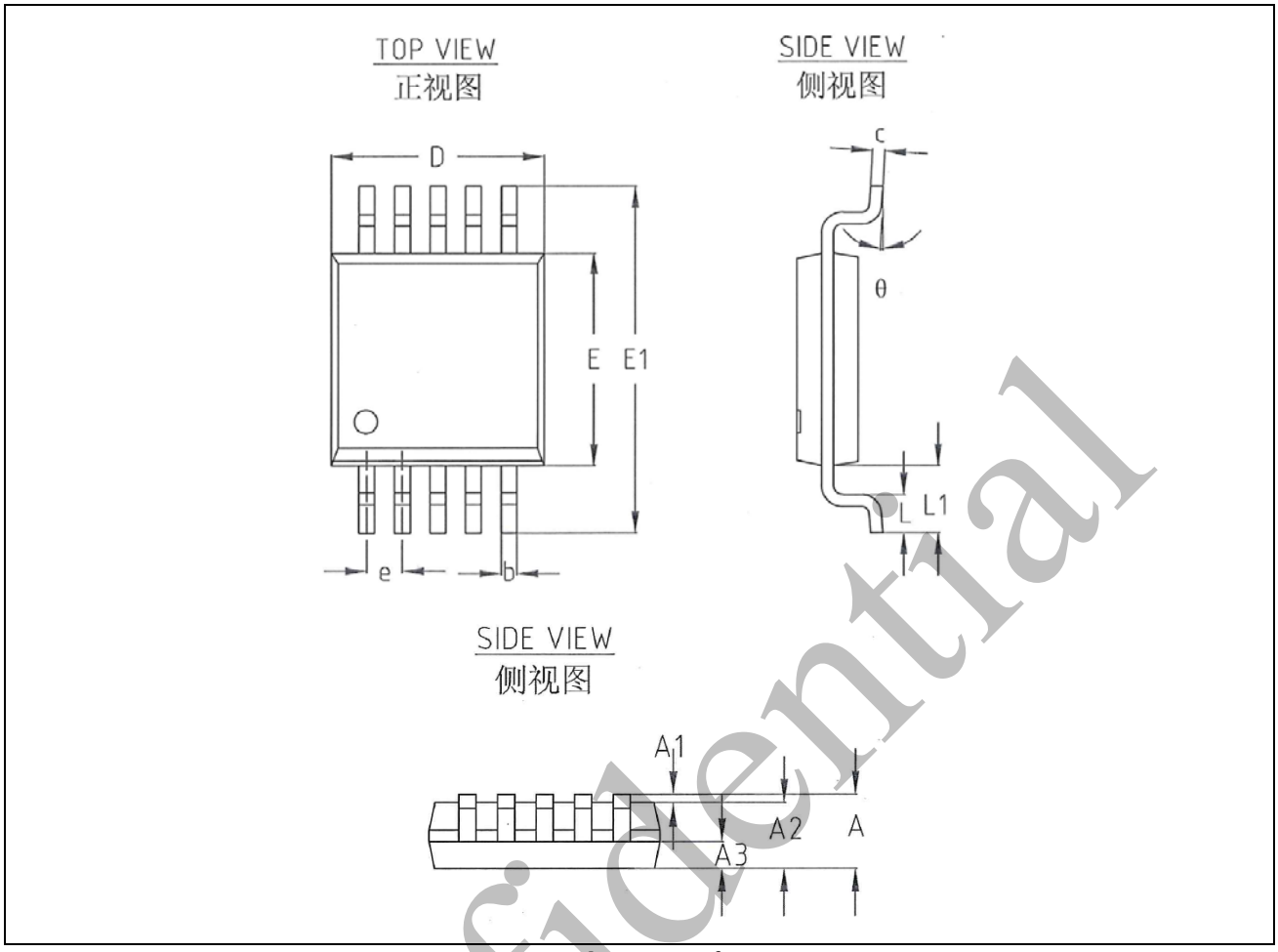


Figure 7-4 Package View for MSOP10

Table 7-2 Package Dimension for MSOP10

SYMBOL	MIN（mm）	NOM（mm）	MAX（mm）
A	-	-	1.10
A1	0.05	-	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18	-	0.26
c	0.15	-	0.19
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
e	0.50BSC		
L	0.40	-	0.70
L1	0.95REF		
Ø	0	-	8°

Abbreviation

ADC	Analog-to-Digital Converter
BOD	Brown-out Detector
CPU	Central Processing Unit
ESD	Electro-Static discharge
GPIO	General-purpose I/O
HXTAL	External high speed crystal oscillator
I2C	Inter-Integrated Circuit
LVR	Low Voltage Reset
LXTAL	32.768 kHz external low speed crystal oscillator
MCU	Micro Control Unit
MISO	Master input slave output
MOSI	Master output slave input
PLL	Phase Locked Loop
POR	Power-on Reset
PWM	Pulse Width Modulation
RCH	32MHz internal high speed oscillator
RCL	32.768kHz internal low speed oscillator
RF	Radio frequency
EEPROM	Electrically Erasable Programmable read only memory
RSSI	Received Signal Strength Indication
SoC	System on chip
SPI	Serial Peripheral Interface
SRAM	Static random access memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver/Transmitters
WDT	Watchdog Timer

Revision History

Version	Date	Content
1.0	Nov. 2025	Initial
1.1	Nov. 2025	Update the partnumber. Add the 4.3.
1.2	Dec. 2025	Update the partnumber and the Pin Information.
1.3	Jan. 2026	Add PAN2711P3CA, PAN2711R3BA and PAN2712P3DA.
1.4	Feb. 2026	Update the SRAM of the PAN2711 and PAN2712. Update the partnumber. Update the *Drive level* in Clock Characteristics. Add the SSOP24 package.

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