PAN2416AF

Technology Reference Manual

2.4GHz RF Transceiver SOC
V1.0

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2.4GHz RF Transceiver SOC

General Description

PAN2416AF is an OTP-based 2.4GHz Transceiver SOC. It is designed for operation in the world wide ISM frequency band at 2.400~2.483GHz, integrating radio frequency (RF) transmitter and receiver, frequency synthesizer, crystal oscillator, baseband GFSK modem, Low power MCU,and so on,supporting one to multiple network and communication with ACK.TX power, frequency channel, and data rate can be set by SPI. The user issues instructions through the MCU's I / O port to the chip, the chip automatically send and receive configuration to communicate, and according to the response information automatically determine whether the data transmission / reception is successful, to re-send, packet loss, continue to send and wait and other operations. TX power, frequency channel, and data rate can be set.PAN2416AF requires a small number of peripheral devices, support single-layer / double-layer printed circuit board program.

Main Features

1、Low power
- 19mA TX at 2dBm output power； 15mA RX at 2Mbps air data rate； 2uA in power down.

2、Low Cost BOM
- Few external components.5 Capacitors, One crystal oscillator
- Support double or single layer PCB design, you can use the printed circuit board microstrip antenna or wire antenna.
- Easy to use by configuring a small number of parameter registers that chip within part of the link layer of the communication protocol.

3、High Performance
- -91/-87/-83dBm@250K/1M/2M bps;Programmable Output Power Up to 8dBm;
- the receiver selectivity is better, high degree of adjacent inhibition.

4、Integrated the MCU module
- OTP：4K×16Bit；
- RAM：176×8Bit；

MCU embedded watchdog timer, LVR module and so on.

Other Features

4 wire SPI port	Support Data whitening and CRC
Support 32 and 64 byte payload length	SOP14 package
1M / 2Mbps:Support±40ppm crystal 250kbps: Support ±20ppm	Operating voltage：2.2~3.3V Operating temperature range：-40~+85℃
GFSK Modulation	Support automatic reply and automatic retransmission

Support RSSI detector	8 GPIO
Interrupt source	Three Timer

Application

Wireless mouse	Remote control of set-top box
Wireless gamepad	Remote controlled toys
Remote controller	Smart home set

Revision	Date	Description	Related documents
V1.0	2017. 11	Draft	

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1. Product Naming Rules

1.1 PAN2416AF naming rules

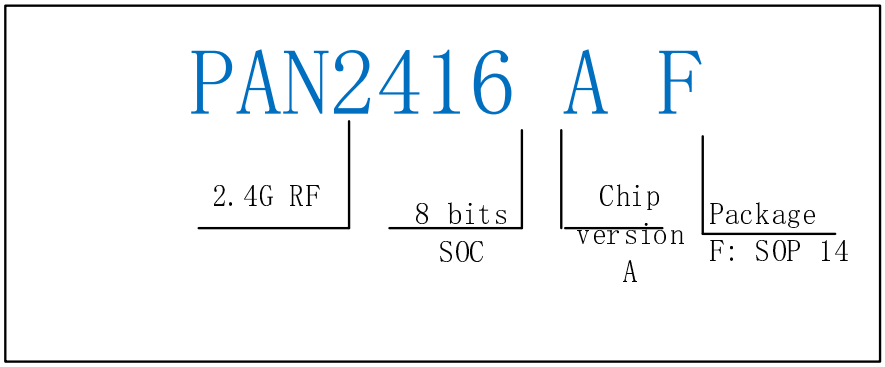


Figure 1.1 PAN2416 serials naming rules

1.2 PAN2416 serials Production

Table1-1 PAN2416 serials Production

Device name	Version	Package Type
PAN2416AV	A	V：SOP16
PAN2416AF	A	F：SOP14

2. Electrical characteristics

Table 2-1 PAN2416AF RF electrical characteristics

Symbol	Condition (VCC = 3V±5%， TA=25℃)	Parameter			Unit
		Min	Typ	Max	
ICC	Sleep		2		uA
	Standby 1		30		uA
	Standby 3		650		uA
	Standby 2		780		uA
	TX at -35dBm output power		9		mA
	TX at -20dBm output power		9.5		mA
	TX at 0dBm output power		16		mA
	TX at 2dBm output power		19		mA
	TX at 8dBm output power		30		mA
	TX at 13dBmoutput power		66		mA
	RX at 250Kbps		15		mA
	RX at 1Mbps		15.5		mA
	RX at 2Mbps		16.5		mA
General RF					
f_{OP}	Operating frequency	2400		2483	MHz
PLL_{res}	PLL Programming resolution		1		MHz

f_{XTAL}	Crystal frequency		16		MHz
DR	Data rate	0.25		2	Mbps
Δf_{250K}	Frequency deviation @250Kbps		125	150	KHz
Δf_{1M}	Frequency deviation @1Mbps		160	300	KHz
Δf_{2M}	Frequency deviation @2Mbps		320	550	KHz
FCH_{250K}	Channel spacing @250Kbps		1		MHz
FCH_{1M}	Channel spacing @1Mbps		1		MHz
FCH_{2M}	Channel spacing @2Mbps		2		MHz
Transmitter					
PRF	Typical output power	2	8	8	dBm
PRFC	Output Power Range	-35		8	dBm
PBW1	20dB Bandwidth for Modulated Carrier（250Kbps）		500		KHz
PBW2	20dB Bandwidth for Modulated Carrier（1Mbps）		1		MHz
PBW3	20dB Bandwidth for Modulated Carrier（2Mbps）		2		MHz
Receiver（Note1）					
RX_{max}	Maximum received signal at <0.1% BER		0		dBm
RXSENS1	Sensitivity (0.1%BER)）@250Kbps		-91		dBm
RXSENS2	Sensitivity（0.1%BER）@1Mbps		-87		dBm
RXSENS3	Sensitivity（0.1%BER）@2Mbps		-83		dBm
Receiver					
C/I_{CO}	C/I Co-channel @250kbps		2		dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I @250kbps		-8		dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I @250kbps		-18		dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I @250kbps		-24		dBc
C/I_{4TH}	4thAdjacent Channel Selectivity C/I 性@250kbps		-28		dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I @250kbps		-32		dBc
C/I_{6TH}	6th Adjacent Channel Selectivity C/I @250kbps		-35		dBc
C/I_{CO}	C/I Co-channel @1Mbps		10		dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I @1Mbps		1		dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I @1Mbps		-18		dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I @1Mbps		-23		dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I @1Mbps		-28		dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I @1Mbps		-32		dBc

C/I_{6TH}	6th Adjacent Channel Selectivity C/I @1Mbps		-35		dBc
C/I_{CO}	C/I Co-channel @2Mbps		10		dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I @2Mbps		-6		dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I @2Mbps		-10		dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I @2Mbps		-22		dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I @2Mbps		-28		dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I @2Mbps		-34		dBc
Operating conditions					
VDD	Supply voltage	2.2	3	3.3	V
VSS	Ground		0		V
V_{OH}	Output high level voltage	VDD-0.3		VDD	V
V_{OL}	Output low level voltage	VSS		VSS+0.3	V
V_{IH}	Input high level voltage	VDD-0.3		VDD	V
V_{IL}	Input low level voltage	VSS		VSS+0.3	V

* Note: In the channels, such as 2416 and 2432 MHz, integer times of 16MHz crystal, receiver sensitivity degrades about 2dB; and modulation quality of the emission signal (EVM) falls by 10%.

* Note: In 250KBps mode, it should not be more than 16 bytes of payload length, because of frequency drift in open-loop transmition.

3. Absolute maximum ratings

Table3-1 PAN2416AF absolute maximum ratings

Symbol	Condition	Parameter			Unit
		Min	Typ	Max	
maximum ratings					
VDD	Supply voltage	-0.3		3.6	V
V_I	Input voltage	-0.3		3.6	V
V_O	Output voltage	VSS		VDD	
Pd	Total Power Dissipation （TA=-40℃~85℃）			300	mW
T_{OP}	Operating Temperature	-40		85	℃
T_{STG}	Storage Temperature	-40		125	℃

* Note: Exceeding one or more of the limiting values may cause permanent damage to PAN2416AF.
* Caution: Electrostatic sensitive device, comply with protection rules when operating.

4. Block diagram

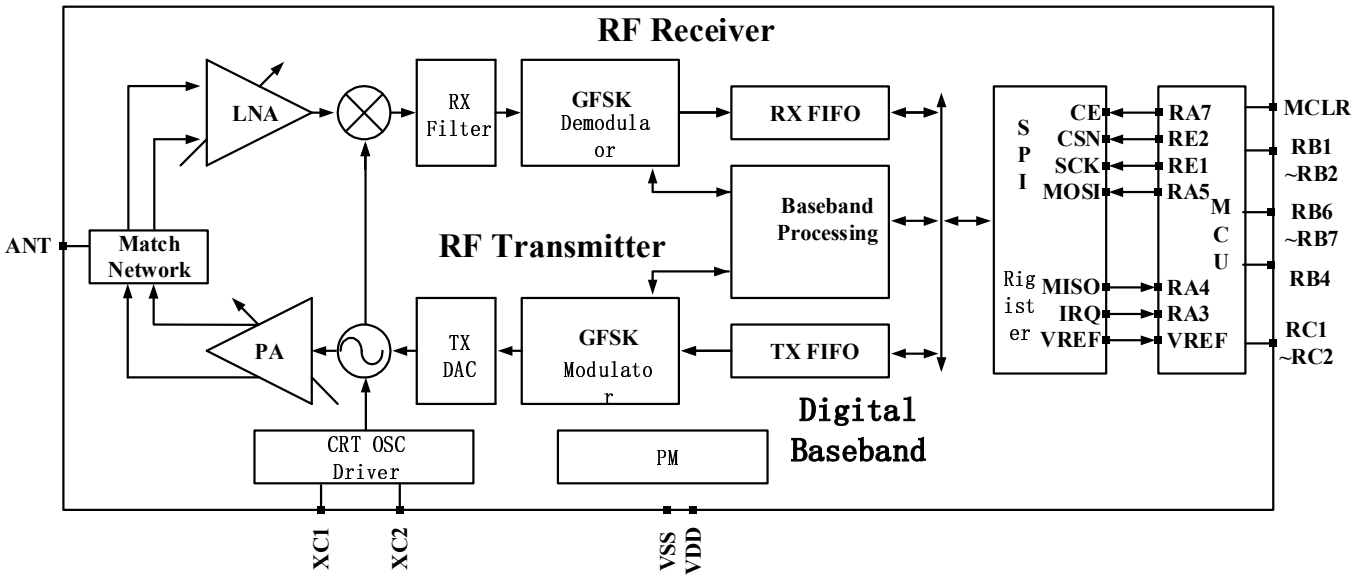


Figure4.1 PAN2416AF block diagram

5. Pin definition

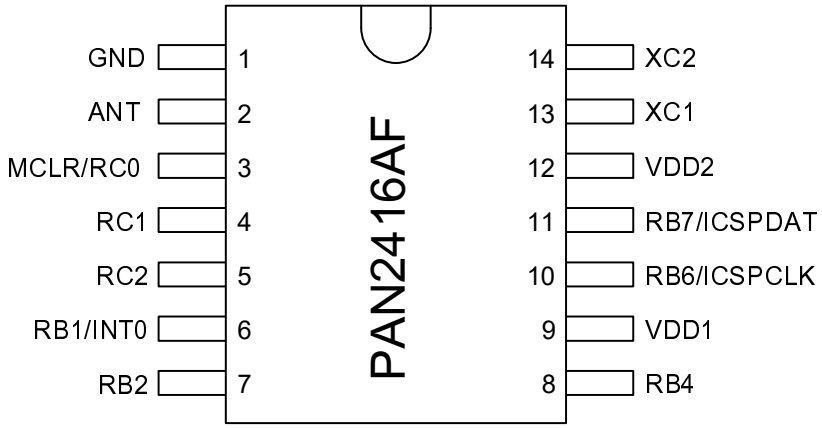


Figure 5.1 PAN2416AF Pin definitions

Table5-1 Pin Description

PIN	Name	IO type	Function
1	GND	P	GND
2	ANT	I/O	Antenna interface
3	RC0	I/O	Input, Open drain output
	MCLR	I	Programming High Voltage input
4	RC1	I/O	Input, Input with Pull-up resistor, Push-pull output
5	RC2	I/O	Input, Input with Pull-up resistor, Push-pull output
6	RB1	I/O	Input, Input with Pull-up resistor, Push-pull output
	INT0	O	Extenal Interrupur input
7	RB2	I/O	Input, Input with Pull-up resistor, Push-pull output
8	RB4	I/O	Input, Input with Pull-up resistor, Push-pull output
9	VDD1	P	Power Supply
10	RB6	I/O	Input, Input with Pull-up resistor, Push-pull output
	ICSPCLK	I	Programming Clock
11	RB7	I/O	Input, Input with Pull-up resistor, Push-pull output
	ICSPDAT	I/O	Programming Data
12	VDD2	P	Power Supply
13	XC1	I	Crystal Pin 1
14	XC2	O	Crystal Pin 2

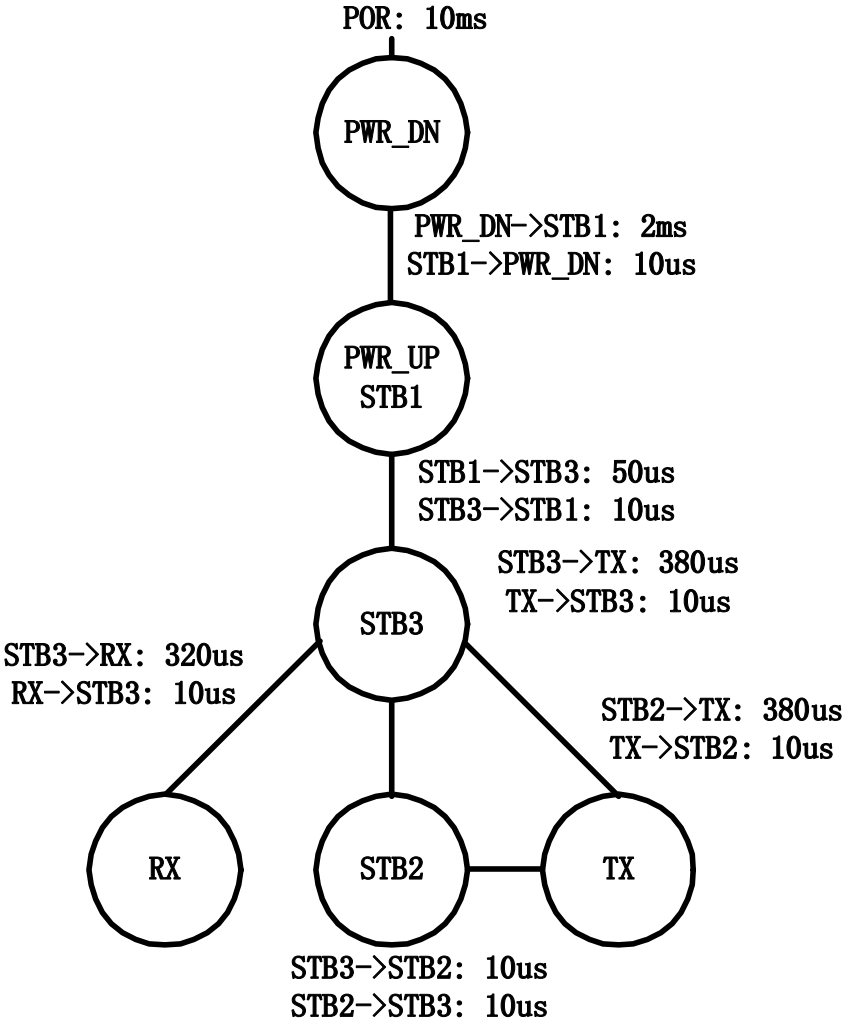
Table5-2 Inter connection of RF and MCU

Description	RF SPI	Direction	MCU SPI
Chip Mode Select Signal	CE	→	RA7
SPI Chip Select	CSN	→	RE2
SPI SPI Clock	SCK	→	RE1
SPI Data Input	MOSI	→	RA5
SPI Data Output	MISO	←	RA4
Interrupt pin	IRQ	←	RA3
Reference Voltage	VREF	←	VREF

6. Operational Modes

This chapter describes PAN2416AF all kinds of working mode, and is used to control the chip into the working mode of method. PAN2416AF own state machine is controlled by chip internal registers configuration values and external signal pin.

Figure 6.1 is PAN2416AF working state diagram, said six working mode between jump PAN2416AF in VDD is greater than 2.2 V to begin to work properly into sleep mode, the MCU can be sent via SPI configuration commands and CE pin into the other five state.



Figue6.1 working status

Table 6-1：Control BIT and function description.

Table 6-1 Control BIT and function description

MODE	PWR_DN	STB1	STB3	STB2	RX	TX
CONTROL BIT						
PWR_UP	0	1	1	1	1	1
EN_PM	0	0	1	1	1	1
CE	0	0	0	1	1	1
PRIM_RX	X	X	X	0	1	0
FUNCTION DESCRIPTION						

SPI operation	√	√	√	√	√	√
Keep register value	√	√	√	√	√	√
Crystal oscillator work	X	√	√	√	√	√
Crystal oscillator output	X	X	X	√	√	√
Main power management work	X	X	√	√	√	√
TX work	X	X	X	X	X	√
RX work	X	X	X	X	√	X

7. DATA FIFO

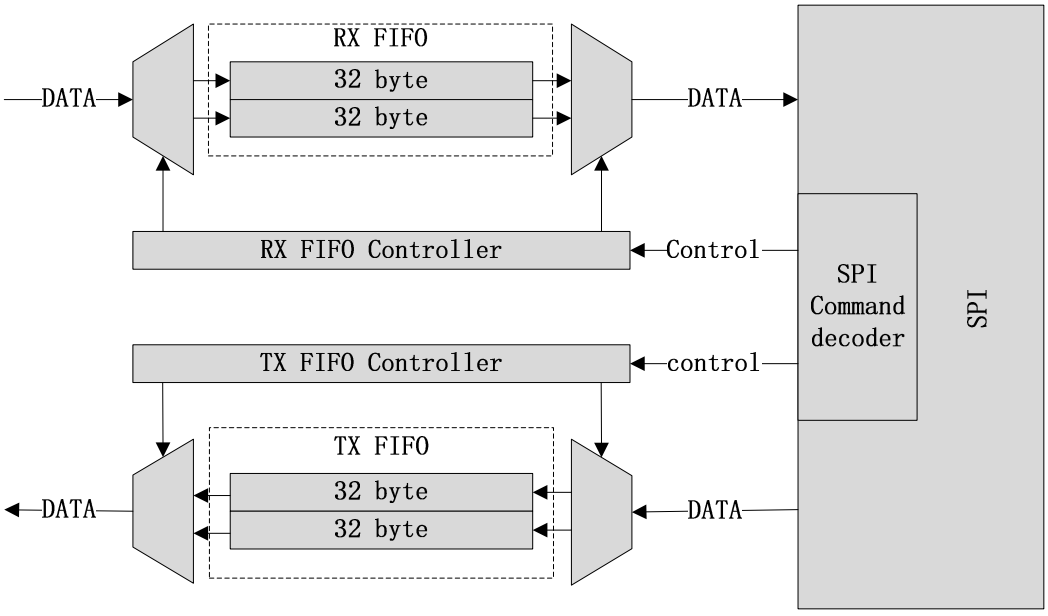


Figure7.4 FIFO block diagram

The PAN2416AF contains TX FIFO, RX FIFO. It is sent via SPI read/write command. It writes TX FIFO in TX mode by W_TX_PAYLOAD and W_TX_NO_ACK instructions. If MAX_RT interruption, data will be cleared in the TX FIFO. It reads PAYLOAD in RX FIFO in receiving mode by R_RX_PAYLOAD, and it reads the length of the PAYLOAD by R_RX_PL_WID instruction. FIFO_STATUS register indicates FIFO states.

7.1 IRQ PIN

In the status register TX_DS RX_DR or MAX_RT is 1, report and the corresponding interrupt enable bit is 0, IRQ pins interrupt trigger. The MCU writes 1 to the corresponding interrupt source, clear the interrupt. IRQ pins interrupt trigger can be blocked or enabled, report by setting the interrupt enable bit is 1, ban IRQ pins interrupt triggered.

8. SPI CONTROL

The PAN2416AF is controlled by SPI port for read and write register, and command. The PAN2416AF is a slave terminal, SPI transfer rate depends on the MCU interface speed, and the maximum data transfer rate is 8 MBps.

SPI interface is a standard SPI interface are shown in table 5, you can use the general I/O for MCU simulation SPI interface. CSN pin to 0, SPI interface instructions to be performed. From 1 to 0 a CSN pin changes execute one instruction. After the change from 1 to 0 CSN pin can be read by MISO status register contents.

Table 8-1 SPI port

PIN	I/O DIRECTION	FUNCTION DESCRIPTION
CSN	Input	SPI Chip Select
SCK	Input	Clock
MOSI	Input	Serial Data Input
MISO	Output	Serial Data Output

8.1 SPI Commands

<Command word: MSBit to LSBit (one byte)>
<Data bytes: LSByte to MSByte, MSBit in each byte first>

Table8-3 SPI command format

COMMAND	COMMAND WORD (BINARY)	DATA BYTES	OPERATION
R_REGISTER	000A AAAA	1 to 5	Write registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
W_REGISTER	001A AAAA	1 to 5	Read RX-payload. A read operation starts at byte 0. Payload is deleted from RX FIFO after it is read. Used in RX mode.

R_RX_PAYLOAD	0110 0001	1 to 32/64	Write TX-payload. A write operation starts at byte 0. Used in TX payload.
W_TX_PAYLOAD	1010 0000	1 to 32/64	Flush TX FIFO, used in TX mode
FLUSH_TX	1110 0001	0	Flush RX FIFO, used in RX mode
FLUSH_RX	1110 0010	0	Used for a PTX device, reuse last transmitted payload. Packets are repeatedly retransmitted as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH_TX is executed.
REUSE_TX_PL	1110 0011	0	This write command followed by data 0x73 activates the following features: • R_RX_PL_WID • W_TX_PAYLOAD_NOACK • W_ACK_PAYLOAD This is executable in power down or standby modes only. This write command followed by data 0x8C deactivates the following features:
ACTIVATE DEACTIVATE	0101 0000	1	Read RX-payload width for the top, R_RX_PAYLOAD in the RX FIFO.
R_RX_PL_WID	0110 0000	0	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum two ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle.
W_ACK_PAYLOAD	1010 1PPP	1 to 64	Write Payload to be transmitted, used in TX mode. Disable auto ACK on this packet.
W_TX_PAYLOAD_NOACK	1011 0000	1 to 32/64	SPI command CE internal logic 1, use the command followed by the data 0x00
CE_FSPI_ON	1111 1101	1	SPI command CE internal logic 0, use the command followed by the data 0x00
CE_FSPI_OFF	1111 1100	1	With the command followed by data 0x5A, makes the XN297L into reset and maintain

			With the command followed by data 0xA5, release the XN297 reset and start to work normally
RST_FSPI_HOLD RST_FSPI_RELS	0101 0011	1	No Operation.
NOP	1111 1111	0	Write registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.

The R_REGISTER and W_REGISTER commands can operate on single or multi-byte registers. When accessing multi-byte registers, first read or write the MSBit of LSByte. Terminate the writing before all bytes in a multi-byte register are written, then it leaves the unwritten MSByte(s) unchanged. For example, the LSByte of RX_ADDR_P0 can be modified by writing only one byte to the RX_ADDR_P0 register.

8.2 SPI Timing

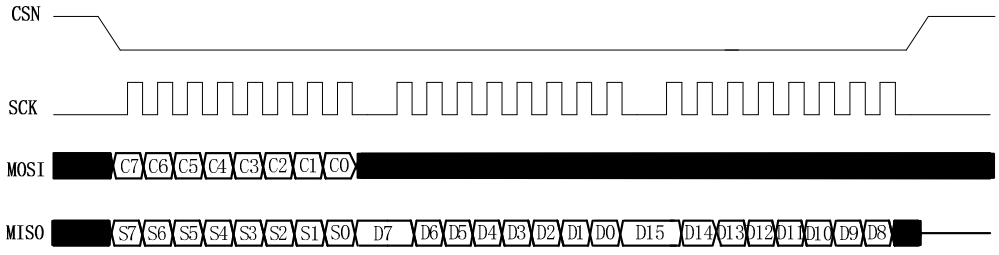


Figure 8.1 SPI read operation

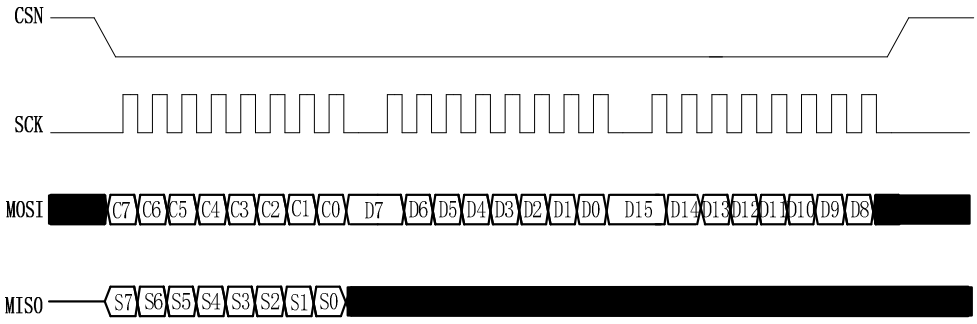


Figure8.2 SPI write operation

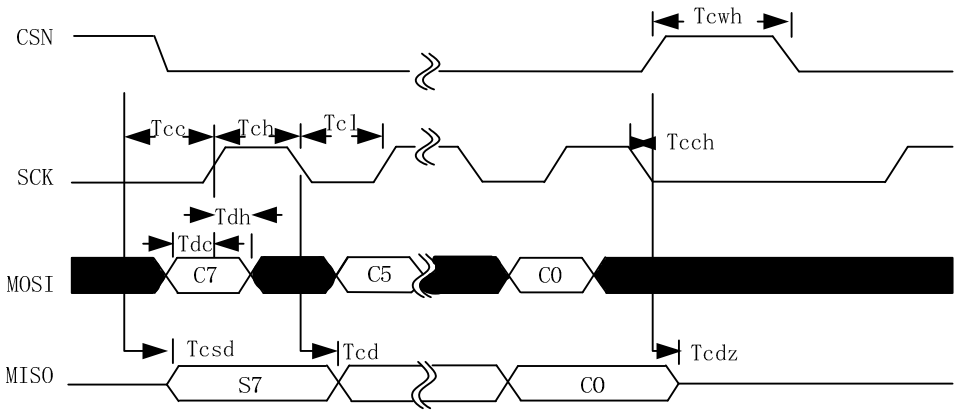


Figure 8.3 SPI NOP timing diagram

9. Packet format description

9.1 Packet format for normal Burst

Table 10-1Packet format for normal burst

Table10-1 Packet format for normal burst

Preamble (3 byte)	Address (3~5 byte)	Payload (1~32/64 byte)	CRC (0/2 byte)

It can choose Address and Payload part to scramble, according to scrambler configuration bits.

9.2 Packet format for Enhanced Burst

Table 10-2 Packet format for enhanced burst

Table 10-2 Table Packet format for enhanced burst

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			Payload (1~32/64 byte)	CRC (0/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)		

It can choose Address, Package control field and Payload part to scramble, according to scrambler configuration bits.

9.3 Packet format for Enhanced Burst ACK

Table 10-3 packet format for enhanced burst ack

Table 10-2 Table Packet format for enhanced burst ACK

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			CRC (0/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)	

It can choose Address, Package control field to scramble, according to scrambler configuration bits.

10. MCU PRODUCT OVERVIEW

10.1 Features

- Memory
  OTP: 4K×16Bit
  RAM: 176×8Bit
- 8 Stack
- 68 Instruction
- LVR
- Interrupt
  3 timer
  RB port external interrupt
  Other interrupt
- Operating Voltage Range
  2.5V—3.3V@8MHz
  2.2V—3.3V@4MHz
  Operating Temp. Range: -40℃—85℃
- Internal Oscillator Frequrency
  RC Oscillator: 8MHz
- Instruction period (one cycle or two)
- WDT timer
- Table Look-up Function
- 3 timer
  8bit timer TIMER0，TIMER2
  16bit timer TIMER1

10.2 SYSTEM BLOCK DIAGRAM

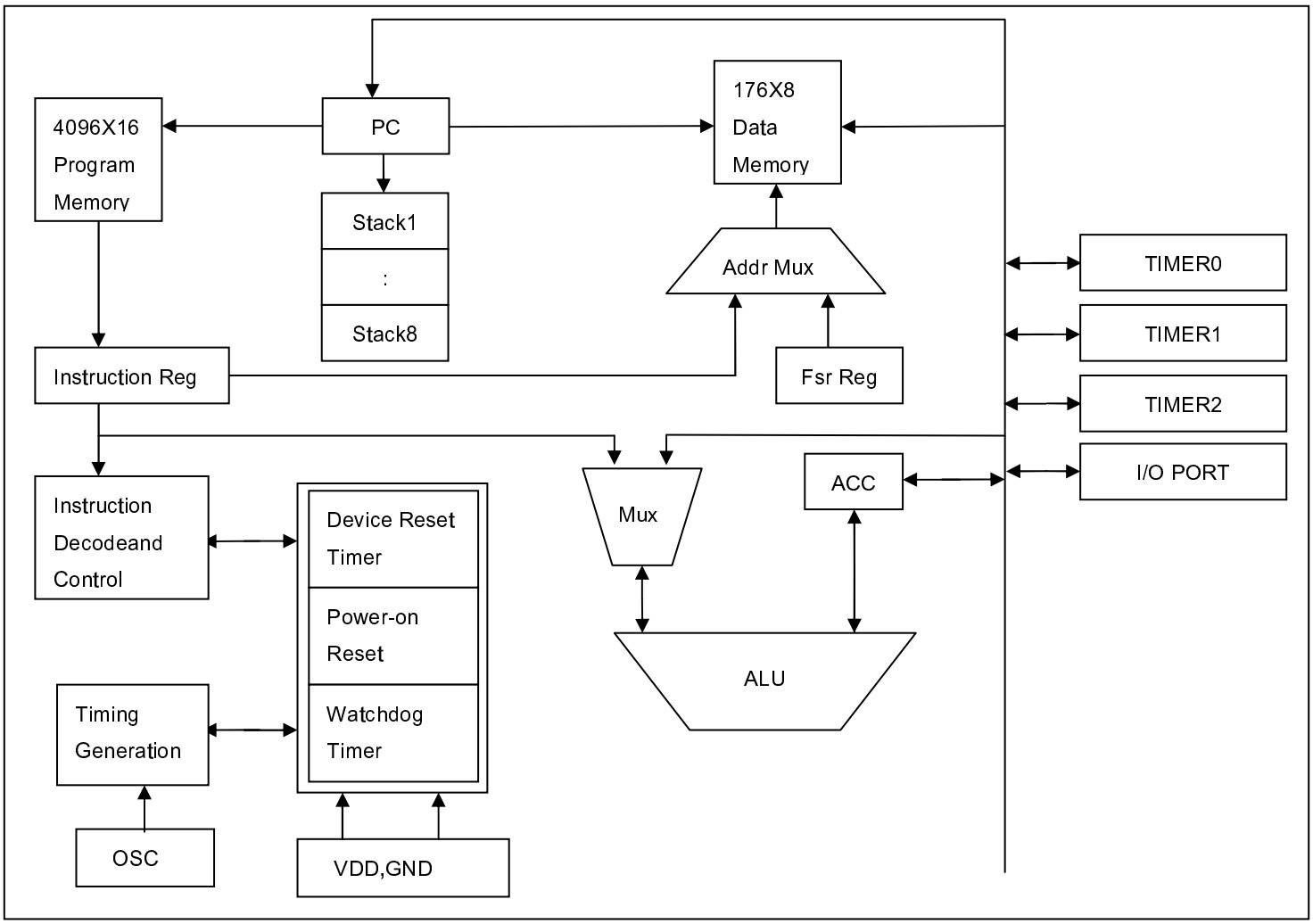


Diagram 11.2 MCU SYSTEM BLOCK DIAGRAM

10.3 SYSTEM CONFIGURATION REGISTER

System configuration register (CONFIG) is OTP option of MCU initial condition. It can be written by SCMCU Writer only, and users cannot access or manipulate it, it includes:

1、OSC(oscillator option)

◆ INTRC Internal RC oscillator

2、WDT(Watchdog Option)

◆ ENABLE Enable watchdog timer

◆ DISABLE Disable watchdog timer

3、PROTECT(Encryption)

◆DISABLE OTP code unencrypted

◆ENABLE OTP code encrypted, the value read after encryption is uncertain.

4、LVR_SEL(Low Voltage Regulator Selection)

◆1.8V
◆2.5V

10.4 IN-CIRCUIT SERIAL PROGRAMMING

PAN2416 products are programmable in the designated application circuit over the following 5 lines:

- Power line
- Ground line
- Data line
- Clock line
- Program voltage line

It allows user to assemble circuit boards by using unprogrammed MCU and program MCU before delivery. Thus the latest version of program can be written in MCU.

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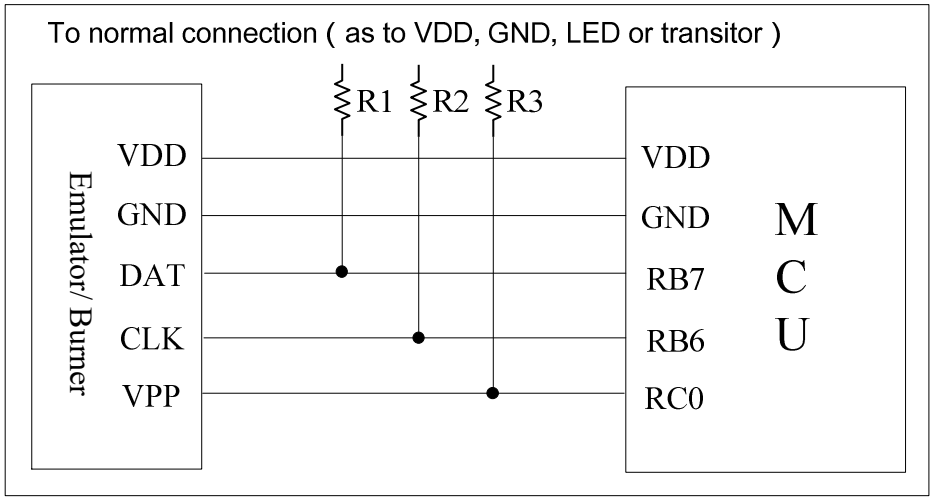


Diagram 11.2 Typical In-circuit Serial Programming Method

In the above diagram, R1, R2 and R3 are electric isolation devices. Usually they are resistors and the value is as below: R1≥4.7K, R2≥4.7K, R3≥30K.

11. CENTRAL PROCESSING UNIT (CPU)

11.1 INTERNAL MEMORY

11.1.1 PROGRAM INTERNAL MEMORY

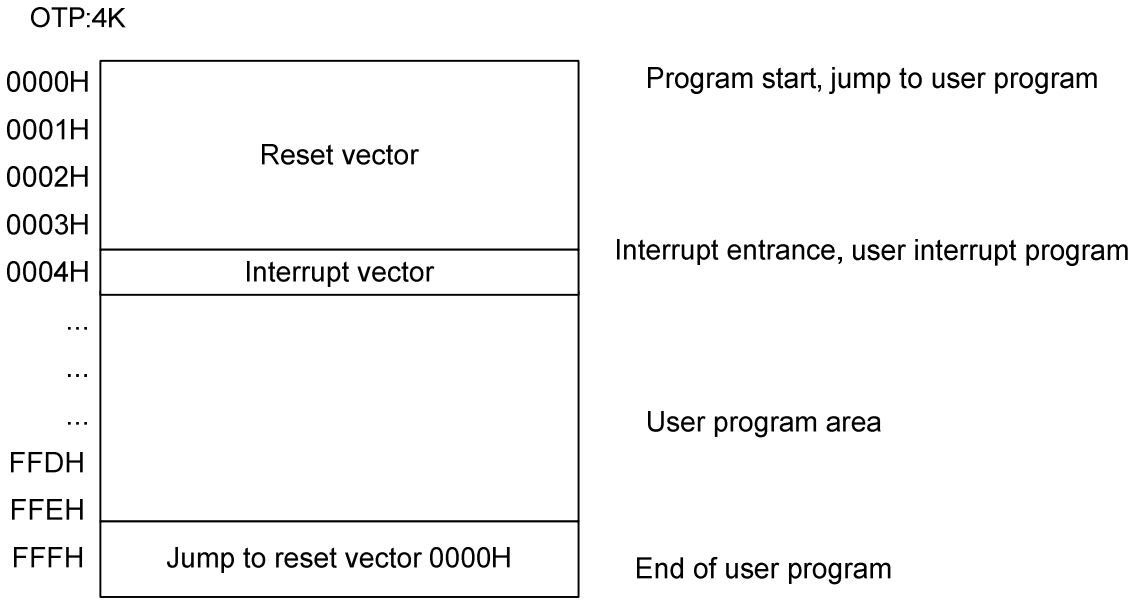


Diagram12.1 PAN2416AV 4K-FLASH Address Table

11.1.2 Data Registor

	地址		地址		地址		地址
INDF	00H	INDF	80H	INDF	100H	INDF	180H
TMR0	01H	OPTION_REG	81H	TMR0	101H	OPTION_REG	181H
PCL	02H	PCL	82H	PCL	102H	PCL	182H
STATUS	03H	STATUS	83H	STATUS	103H	STATUS	183H
FSR	04H	FSR	84H	FSR	104H	FSR	184H
PORTA	05H	TRISA	85H	WDTCON	105H	----	185H
PORTB	06H	TRISB	86H	PORTB	106H	TRISB	186H
PORTC	07H	TRISC	87H	----	107H	----	187H
----	08H	----	88H	----	108H	----	188H
PORTE	09H	TRISE	89H	----	109H	----	189H
PCLATH	0AH	PCLATH	8AH	PCLATH	10AH	PCLATH	18AH
INTCON	0BH	INTCON	8BH	INTCON	10BH	INTCON	18BH
PIR1	0CH	PIE1	8CH	----	10CH	----	18CH
----	0DH	----	8DH	----	10DH	----	18DH
TMR1L	0EH	----	8EH	----	10EH	WPUA	18EH
TMR1H	0FH	OSCCON	8FH	----	10FH	WPUC	18FH
T1CON	10H	OSCTUNE	90H	TABLE_SPH	110H	----	190H
TMR2	11H	----	91H	TABLE_SPL	111H	----	191H
T2CON	12H	PR2	92H	TABLE_DATAH	112H	----	192H
----	13H	----	93H	----	113H	----	193H
----	14H	----	94H	----	114H	----	194H
CCPR1L	15H	WPUB	95H	----	115H	----	195H
CCPR1H	16H	IOCB	96H	----	116H	----	196H
CCP1CON	17H	----	97H	----	117H	----	197H
----	18H	----	98H	----	118H		198H
----	19H	----	99H	----	119H	----	199H
----	1AH	----	9AH	WPUE	11AH		19AH

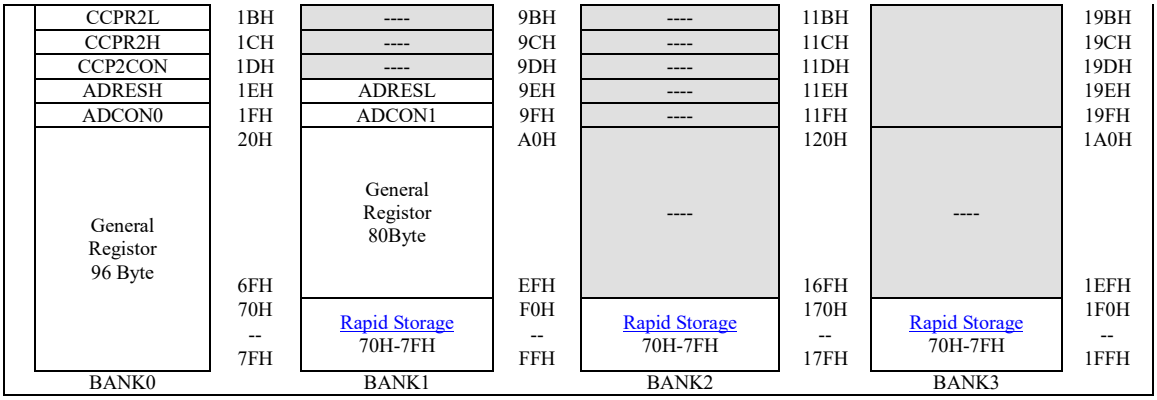


Diagram 12.5 PAN2416AV Data Registor list

12. Apllication examples of fewer external components

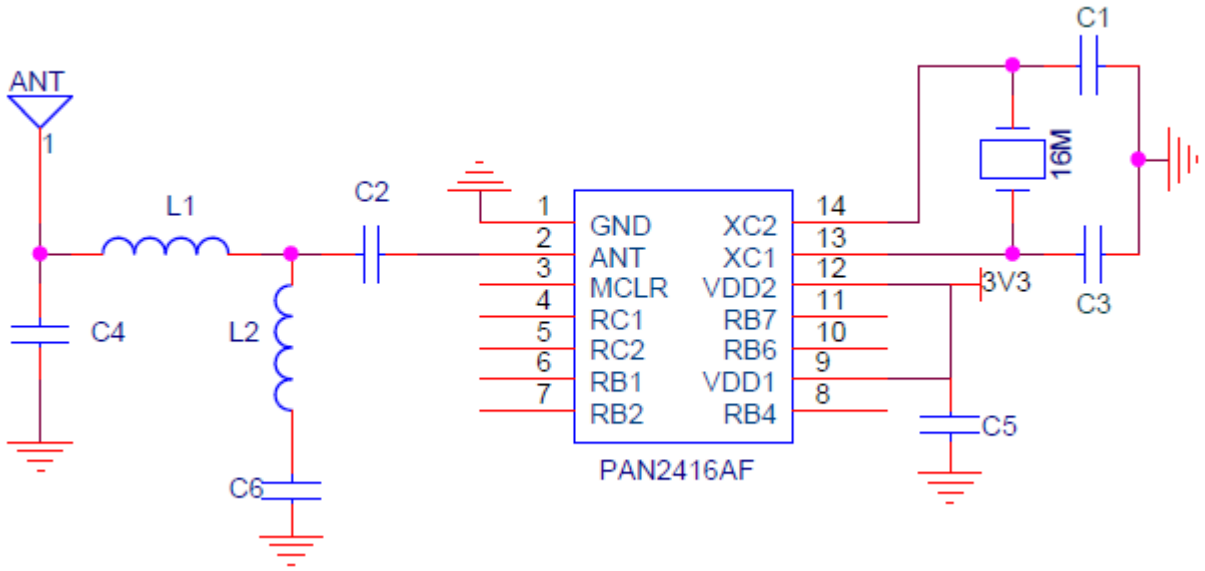


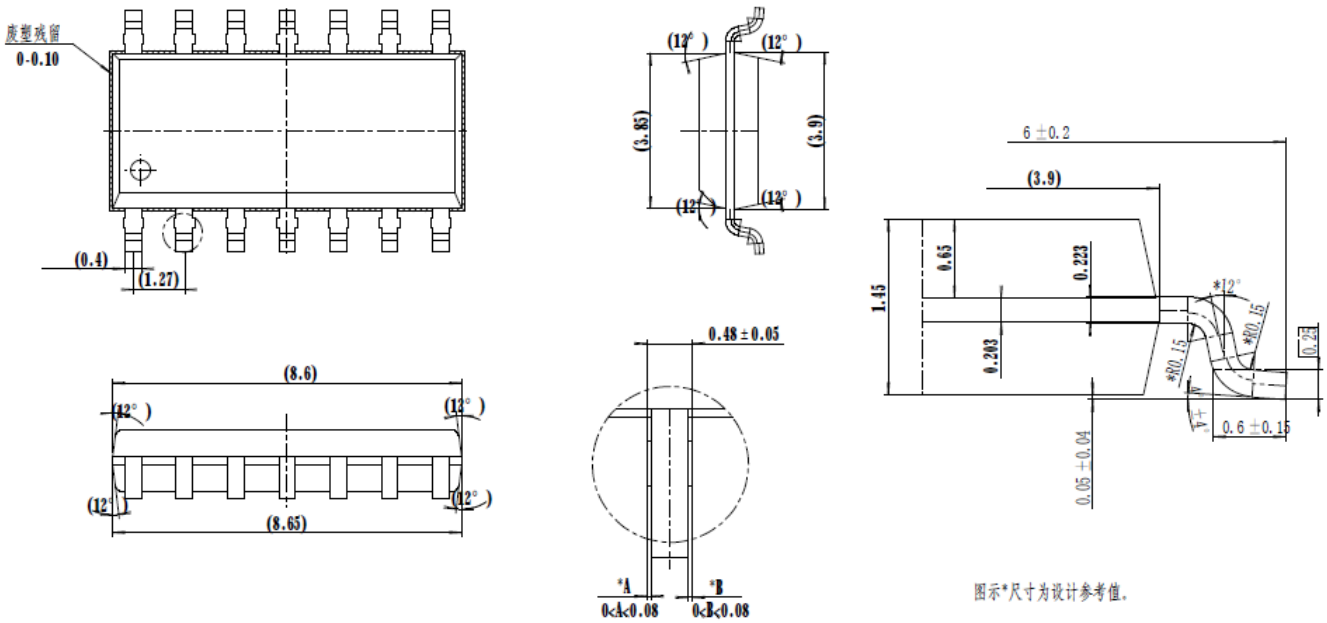
Figure11 PAN2416AF Apllication examples of fewer external components

Notes：RF matching part of the test for the single / double-sided test transmitter and receiver can be certified through the safety certification.

BOM	Notes
C1 / C3	Resonant capacitor，adjusting ，Optional scope 15~36pF
C5	0.1uF
C2	Recommended 3.3pF，Optional scope2~4pF
L1	5.6nH
L2	2.2nH
C4	0.5pF
C6	0.5pF

13. Package Size

Figure 22.1 package size



14. Connection

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